

Fast Block-Wise V_{DD} -Hopping Scheme

許 螢 雪
Yingxue Xu

宮 崎 隆 行
Takayuki Miyazaki

川 口 博
Hiroshi Kawaguchi

桜 井 貴 康
Takayasu Sakurai

東京大学 生産技術研究所
Institute of Industrial Science, University of Tokyo

1. Introduction

As the CMOS IC's are becoming faster and more complex, the desire for low power designs is increasing continuously. Among a great number of proposals to reduce the power consumption, the V_{DD} -hopping scheme has been demonstrated to achieve power reduction up to 3/4[1]. In this paper, the block-wise V_{DD} -hopping scheme applied to a practical chip was simulated to find its transient characteristics and how the V_{DD} line resistance and decoupling capacitance affect the delay.

2. Simulation of V_{DD} -Hopping Scheme

The block schematic of simulation is shown as Fig.1. Blocks in a chip are connected to the fixed V_{DD} (V_{FIXED}) and the hopping V_{DD} (V_{DDB}), respectively. The IN-signal is generated from a feedback loop circuit which employs two comparators to make the oscillation between V_{DDH} and V_{DDL} , and the bufferings make overlaps to prevent two p-MOSFETs from being off at the same time. The model for HSPICE simulation is a Hitachi 0.18 μm CMOS process with supply voltage of 1.8V.

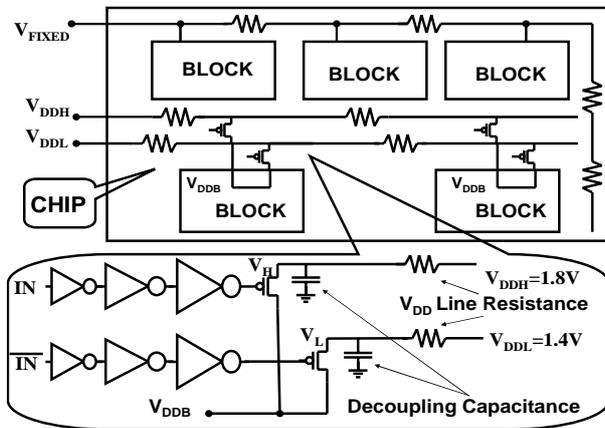


Fig.1. V_{DD} -hopping circuit for simulation.

Assuming that the V_{DD} line resistance equals to 3 Ω which is the approximated value of a 50 μm interconnect wire from V_{DD} outside to a block in the center of a chip, and the gate capacitance of the load circuit is about 120pf. Fig.2 illustrated the waveforms of V_{DD} and V_H when the decoupling capacitance is set to 0pf and 100pf respectively. With the same input IN, there is a difference of 0.5ns between them in the delay (defined as 50% fall to 90% rise). Furthermore the curves show that the V_{DDB} is very close to V_H which also means that the RC delay dominates.

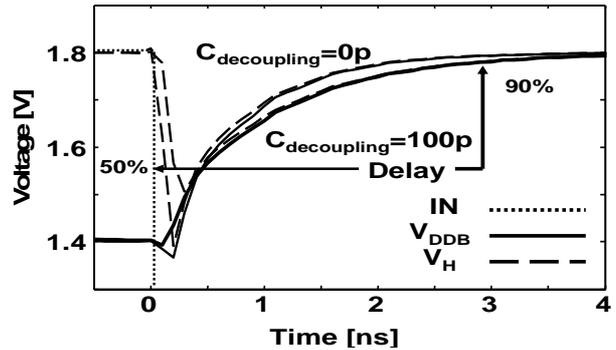


Fig.2. Waveforms of V_{DD} and V_H .

Then the V_{DD} line resistance and decoupling capacitance's effects on the delay are also examined as shown in Fig.3. It is obvious that the delay is in proportion to the V_{DD} line resistance.

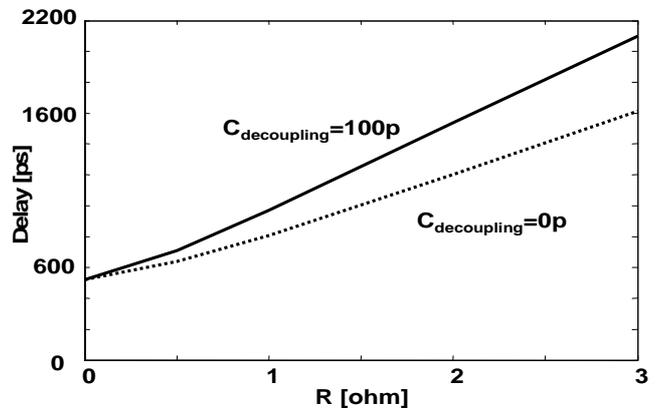


Fig.3. The effect of R and C on delay.

3. Conclusion

The decoupling capacitance degrades the speed of V_{DD} -hopping while the V_{DD} line resistance dominates the delay. If V_{DD} line resistance is negligible, possibly using area pad and thick lines in interposer packages, the V_{DD} -hopping delay will be less than 0.5ns in 0.18 μm technology node and even 0.1ns in 65nm node.

4. References

[1] H. Kawaguchi, et al, "An LSI for V_{DD} -Hopping and MPEG4 System Based on the Chip," ISCAS, pp.918-921, May 2001.