V$_{DD}$-Hopping Accelerators for On-Chip Power Supply Circuit to Achieve Nano-Second Order Transient Time

Kohei Onizuka$^*$, Hiroshi Kawaguchi$^{**}$, Makoto Takamiya$^*$ and Takayasu Sakurai$^{**}$

$^*$) Institute of Industrial Science and $^{**}$) Center for Collaborative Research, University of Tokyo

4-6-1 Komaba, Meguro-ku, Tokyo, 153-8505, JAPAN

$^{**}$) Department of Computer and Systems Engineering, Kobe University

1-1 Rokkodai, Nada, Kobe, 657-8501, Japan

Abstract

A V$_{DD}$-hopping accelerator for on-chip power supply circuits is proposed and the effectiveness of the accelerator circuit is experimentally verified. The quick dropper with the linear regulator enables nano-second order transient time in on-chip distributed power supply systems. The measured transition time is less than 5ns with load circuit equivalent to 25k logic gates in 0.18-μm CMOS. This is to be compared with the case without the accelerator of the order of μs and thus the acceleration by two orders of magnitude is achieved. Extensions of the basic approach are also discussed including implementation of the quick dropper for a switching DC-DC converter, the control stability improvement, automatic timing generation and the parasitic element effects of the power lines.

Index Terms

V$_{DD}$-hopping, power supply, linear regulator, DC-DC converter, mirror-delay, parasitic elements.
I. Introduction

System-on-a-Chip (SoC) and System-in-a-Package (SiP) have become major integration technologies in recent years. They are often used for integrating various types of circuit blocks like MPU, DRAM, SRAM, ROM, logic and analog circuits on a chip or in a package. The optimum and/or required supply voltages ($V_{DD}$) for these types of circuit blocks differ among themselves. Fig.1 shows the $V_{DD}$ trends of precision analog/RF, performance analog/RF, high performance logic and low-power logic with the design rule trends which are extracted from the International Technology Roadmap for Semiconductors (ITRS) 2005[1]. Thus, integrating different types of circuit block needs various local $V_{DD}$ values in an SoC and an SiP. Supplying many different voltages from outside the package can be one solution as shown in Fig.2(a). This method however, gives rise to much overhead in area and brings about the power line integrity issues including IR drop and noise. The distributed on-chip power supply circuits as shown in Fig.2(b) are useful for solving these problems.

On the other hand, for each circuit block, the highest performance may not be required all the time. It has been known that reducing $V_{DD}$ when a required speed is slow decrease the power consumption of a block drastically. To implement this concept, $V_{DD}$-hopping has been introduced, where $V_{DD}$ is changed among discrete levels adaptive to the required performance to reduce power consumption while maintaining the real-time feature [2,3]. Since $V_{DD}$-hopping should be executed for each circuit block, the distributed power supply circuits should have capability of changing the voltage in time.

An on-chip power supply converts the external $V_{DD}$ ($V_{DDEXT}$) into the optimum internal $V_{DD}$ ($V_{DDINT}$) of the load circuit as shown in Fig.3. In the $V_{DD}$-hopping system, the load
circuit should not be used during \( V_{DD} \) transition from one voltage level to another because the load circuit block is not verified its operation between the voltage levels in the test sequence. Therefore, high-speed transition among different levels is important not to steal much time for the voltage hopping.

The load circuit can be approximated as \( R_L \) and \( C_L \) as is shown in Fig.3. \( C_L \) represents all the capacitance associated with the power supply node, including MOSFET’s, interconnections and \( R_L \) represents the current sink capability of the load circuit. When an operation of the load circuit is stopped during the \( V_{DD} \) transition, the circuit draws only leakage current and \( R_L \) increases up to more than kilo-ohm range. Thus, in the transient period of the \( V_{DD} \)-hopping when the load circuit stops operating, there is eventually no path to pull down the internal voltage to the lower level and the transient becomes intolerably long. Fig.3(b) shows an example of an ideal waveform for \( V_{DDINT} \) and the actual waveform. The long transition time steals much time in the \( V_{DD} \)-hopping and hence reduces performance of the system. Added to this, if the transition time is long, it will be difficult to apply to very quick real-time systems such as servomechanism control systems. In this paper, a technique to reduce the transition time, namely a \( V_{DD} \)-hopping accelerator, is proposed and the effectiveness is verified through experiments. In Section II, the basic concept of the accelerator is introduced followed by the implementation of the accelerator for a linear regulator and a switching DC-DC converter in Section III and IV, respectively. Section V and VI are dedicated for discussions and conclusions.

II. Basic concept of \( V_{DD} \)-hopping accelerator

Fig.4 shows the basic concept of the \( V_{DD} \)-hopping accelerator. The PMOS/NMOS
transistor labeled “quick raiser”/”quick dropper” which is added at the output of a distributed voltage regulator on a chip accelerates the V\textsubscript{DD}-hopping process. The schematic waveforms of V\textsubscript{DDINT} with and without the quick raiser/dropper are shown in Fig.5. The transition time depends on the RC time constant of C\textsubscript{L} and the effective resistance of the quick raiser/dropper, R\textsubscript{ON,P}/R\textsubscript{ON,N}. Since the quick dropper charges/discharges C\textsubscript{L} not aiming at V\textsubscript{DDH}/V\textsubscript{DDL} but aiming at much higher/lower voltage of V\textsubscript{AH}/V\textsubscript{AL}, the charging/discharging time is highly accelerated. The acceleration will be achieved without any extra power supply lines, since V\textsubscript{AH} and V\textsubscript{AL} are available as global power grids.

Basically, the acceleration is achieved by aiming at the higher goal than the target value and stopping at the target value. This “aim-high” is the basic concept for the acceleration. In order to quantitatively discuss the speed acceleration by the aim-high, let us introduce the following three parameters: a voltage overdrive factor \( \alpha \), an achievement ratio \( \beta \) and a speed acceleration factor \( \zeta \). Fig.6 shows several fundamental parameters for the case of a quick dropper. These parameters are defined in a similar fashion for the case of a quick raiser. \( \alpha \) indicates the voltage overdrive and is defined as

\[
\alpha = \frac{A}{B} = \frac{V_{AH} - V_{DDL}}{V_{DDH} - V_{DDL}} = \frac{V_{DDH} - V_{AL}}{V_{DDH} - V_{DDL}}.
\]  

(1)

The achievement ratio \( \beta \) is the ratio of the full transition voltage and the actual transition voltage when we say that the goal is achieved. \( \beta \) is needed because it takes forever to get to the goal (V\textsubscript{DDL}) when there is no overdrive.

\[
\beta = \frac{C}{D}.
\]  

(2)

\( \zeta \) shows the hopping-speed improvement with as the aim-high, which is a function of the
overdrive voltage and the achievement ratio as follows.

\[ \zeta = \frac{\ln(1 - \beta)}{\ln\left(\frac{\alpha - \beta}{\alpha}\right)} - 1. \]  

Fig. 7 shows the speed acceleration factor for typical parameters. If the voltage is initially overdriven by 100% and the voltage error of 5% is allowed, that is, the voltage overdrive factor is 2.0 and the achievement ratio is 95%, the speed is accelerated by a factor of 3.65, which is a huge acceleration.

III. V_{DD}-hopping accelerator for linear regulator

A. Circuit topology

To verify the effectiveness of the V_{DD}-hopping accelerator, the quick dropper for a linear regulator is designed and manufactured. Since the linear regulator has no path to pull down the output voltage in principle, the load capacitance is discharged only by the leakage current of the load circuit. Thus the quick dropper works more effectively for the linear regulator compared with a DC-DC switching regulator. Fig. 8 shows the basic circuit and the waveforms of the quick dropper. Generally, the gate width of the quick dropper is large and buffers are needed to drive it and thus there is a delay. Therefore, the quick dropper must be turned off slightly earlier before the V_{DDINT} reaches the final voltage of V_{DDL} because there is delay \( \tau_{OFF} \), in switching off the dropper. In order to take this delay into account, \( V_{REF} \) which sets the voltage at which the driver for the dropper starts the turning-off process should be a little higher than \( V_{DDL} \) as follows.
\[ V_{\text{REF}} = V_{\text{DDL}} e^{\frac{-\tau_{\text{off}}}{R_{\text{off},n} C_L}}. \]  

(4)

\(V_{\text{REF}}\) is supplied from external to the chip for the measurement but self-aligned generation of the timing is also discussed later in this paper. Lines to distribute \(V_{\text{REF}}\) do not give much overhead in area because there is no need to draw current through the line.

Fig. 9 shows the designed quick dropper with the conventional linear regulator in 0.18-\(\mu\)m CMOS. The load circuit is designed to be equivalent to 25k NAND gates. Fig. 10 shows the schematic waveforms for the quick dropper. \(\tau_{\text{on}}\) and \(\tau_{\text{off}}\) signify the delay of the quick dropper driver to turn on and turn off the dropper itself, respectively. To avoid the output voltage ripple like a voltage overshoot and undershoot, a careful tuning of \(V_{\text{REF}}\) is required.

**B. Simulation and measurement results**

Fig. 11 shows the simulated waveforms of the linear regulator with and without a quick dropper using HSPICE. Here, the leakage power is assumed to be 1\% of the dynamic load circuit power. \(V_{\text{DDH}}\) and \(V_{\text{DDL}}\) equal to 2.0V and 1.5V respectively. The transition time is defined the time from the start of the Select_\(V_{\text{DDH}}\) to the time when the \(V_{\text{DDL}}\) trips 95\% of \(V_{\text{DDH}}\)-\(V_{\text{DDL}}\), that is, the achievement factor is 95\%. As seen from Fig. 11, the transition time with the quick dropper is about 3ns while that without the quick dropper is about 0.4\(\mu\)s. This leads to a long wait before the load circuit can be operated. The voltage ripple right after the transition is smaller than 2\% and thus it is possible to start the operation of the load circuit right after the transition. The simulated performance of line regulation \(\Delta V_{\text{DDINT}}\) is smaller than \(\pm0.8\%\) for \(V_{\text{DDEXT}}\) of 2.0\(\pm0.5\)V and \(V_{\text{DDINT}}\) of 1.2V. The simulated performance of load regulation \(\Delta V_{\text{DDINT}}\) is smaller than 5\% for the maximum load current
of 50mA and $V_{DDINT}$ of 1.5V. The performances of line and load regulations simply depend on the linear regulator circuit itself.

A chip microphotograph of the fabricated linear regulator with the quick dropper is shown in Fig. 12. The quick dropper area is 20µm x 20µm, while the linear regulator area is 30µm x 70µm. The area overhead of the quick dropper can be as small as 2% of the load circuit.

Fig.13 shows the measured waveform for $V_{DDINT}$ which coincides well with the HSPICE simulation. It is seen that the transition time from $V_{DDH}$ to $V_{DDL}$ is smaller than 5ns which enables more than two orders of acceleration over the case without the accelerator circuit.

IV. $V_{DD}$-hopping accelerator for switching DC-DC converter

Implementation of the $V_{DD}$-hopping accelerator for a switching DC-DC (buck) converter is presented in this section. The conventional buck converter needs an inductor and a capacitor to filter out the switching ripples of the switching frequency. As technology advances, the switching frequency is increased and on-chip regulator is investigated because the required value of L and C are reduced [4-7]. The energy efficiency of a switching DC-DC converter is higher than that of a linear regulator and the buck converter is considered to be a promising candidate for the future on-chip distributed voltage regulators.

A buck converter with a quick raiser and a quick dropper is shown in Fig.14. A design is carried out assuming 0.18-µm CMOS and the size of the on-chip filter of 2x2mm. The circuit parameters are determined as $L_F=21$nH and $C_F=3$nF and the switching frequency is
set as 150MHz by using optimization theories [8-10]. Fig.15 shows the simulated waveforms of output voltage $V_{DDINT}$ and the inductor current $I_L$ without a $V_{DD}$-hopping accelerator when $V_{DDH}=1.2V$ and $V_{DDL}=0.6V$. Spurious voltage ringing occurs after voltage transitions due to the LC resonance. The transition times to ±5% of the final voltages are 64ns for $V_{DDH}$ to $V_{DDL}$ transition and 37ns for $V_{DDL}$ to $V_{DDH}$ transition.

Fig. 16 shows the control timing of the $V_{DD}$-hopping accelerator for a buck converter. “Output voltage of switching transistors” indicates the output node voltage of switching transistors of a buck converter. The duty ratio of the PWM signal is assumed to change at the falling edge of the PWM signal (dotted line), that is, the chopping clock. The gate voltage of the quick dropper/raiser starts to change at $\tau_N$ and $\tau_P$ before the falling edge of the chopping clock.

Fig. 17 shows the simulated waveforms for the case with the $V_{DD}$-hopping accelerator. The timing offset, $\tau_N$ and $\tau_P$, are set both to 0ns in this case. Transition time is about 25ns both for $V_{DDH}$ to $V_{DDL}$ and $V_{DDL}$ to $V_{DDH}$ transition, which is shorter than the case without the accelerator but the spurious ringing after the transitions is not negligible. If the timing offset, $\tau_N$ and $\tau_P$, are set to 2ns and 2.2ns respectively, the transition time is reduced to 6ns for $V_{DDH}$ to $V_{DDL}$ and 4ns for $V_{DDL}$ to $V_{DDH}$ as is shown in Fig.18. The output voltage is stabilized by limiting the long-term fluctuation of the average inductor current. Thus a careful tuning of the timing offsets is considered to be effective in further reducing the transition time.

V. Discussions

Improved control methodologies in two ways and parasitic element effects of the power lines are discussed in this section.
A. Stability enhancement

The quick dropper shown in Fig.9 requires a proper setting of $V_{\text{REF}}$. When $V_{\text{REF}}$ is set to be lower than the expected value (higher for a quick raiser), the output voltage may overshoot and oscillation may occur because there are two feedback loops, one for the linear regulator and the other for the quick dropper and both loops operate at the same time and independently. The cycle time of the oscillation depends on the total delay of the two feedback loops. On the other hand, the duration of the oscillation is the same as the active period of the quick dropper, which is determined by the Delay circuit in Fig.9. Fig.19 shows the measured and simulated waveforms for the circuit shown in Fig.9 when $V_{\text{REF}}$ is much lower than the proper value, where spurious oscillation is observed. By limiting the activation of the quick dropper only once per transition, the oscillation can be eliminated. Fig.20 shows the improved version of the quick dropper, where the activation is limited to once per transition. The pulse generator1 activates the JK latch and the pulse generator2 inactivates at the end of the quick dropping operation. Fig.21 shows the simulated waveform using HSPICE when $V_{\text{REF}}$ is much lower than the proper value. This one-time control approach is effective not only to the linear regulators but also to other types of DC-DC converters.

B. Self-aligned timing generation

$V_{\text{REF}}$ sets the basis of critical timings for the $V_{\text{DD}}$-hopping acceleration and is assumed to be provided from outside of a package. This is doable since the $V_{\text{REF}}$ does not carry current and the area overhead is small even although the $V_{\text{REF}}$ line is shielded from adjacent signals by using $V_{\text{SS}}$ lines. The adjustment of $V_{\text{REF}}$, however, is critical to the accelerator operation as is explained in Section III. The proper $V_{\text{REF}}$ value is dependent on the load circuit as is
expressed in (4). Again it is doable by adjusting from outside but if the timing signals can be generated on a chip indifferent from the load circuit, the applicability of the circuit in SoC/SiP environments will increase. To address this issue, automatic generation of the timings in a self-aligned manner is considered here.

Fig. 22 shows the concept of the proposed approach. It is possible to approximate the exponential voltage waveform by a linear transition. Therefore, once the delay required from the start of the transition to the half point of the trip to \( V_{DDL} \) is known, the remaining transition time to \( V_{DDL} \) is predictable. The half voltage can be generated by a simple on-chip circuit. \( V_{DDL} \) is to be distributed but it is the same for all the circuit blocks while \( V_{REF} \) is different for each circuit blocks.

Fig. 23 shows the circuit diagram of a quick dropper with the proposed control. The timing sequence shown in Fig. 22 can be implemented by a mirror-delay circuit which consists of two capacitors C1 and C2. Fig. 24 shows the simulated waveforms of the circuit by HSPICE assuming 0.18-µm CMOS with \( V_{DDH}=2.0V \) and \( V_{DDL}=1.2V \).

The mirror-delay circuit works as follows. At the start, both of C1 and C2 are discharged to \( V_{SS} \). Then, charging of C1 is started when the time span of \( \Delta_{ON}+\Delta_{OFF} \) passed. The charging process ends when \( V_{DDINT} \) reaches the middle voltage of \( V_{DDH} \) and \( V_{DDL} \). Then, charging of C2 begins. When the terminal voltage of C1 and C2 gets equal, the turn-off process for the dropper transistor is initiated. In this process, the delay adjustment for \( \tau_{ON}+\tau_{OFF} \) is required to compensate the delay for the driver circuit of the dropper transistor. This can be achieved by a help of a replica circuit as shown in the figure.

Fig. 25 shows the simulated waveforms of \( V_{DDINT} \) when the load capacitance \( C_L \) varies from 15pF to 30pF. It is seen from the figure that the final voltage of \( V_{DDL} \) is achieved for a
wide range of $C_L$ without changing the control circuit itself. Thus the self-aligned feature is verified. It is possible to widen the range of $C_L$ furthermore by using variable capacitors for $C1$ and $C2$ by using multiple capacitors in parallel and a digital control.

**C. Parasitic element effects**

The distributed voltage regulator with a $V_{DD}$-hopping accelerator is supposed to be on a global power grid as shown in Fig.26. There are parasitic RLC components on the global power grid on a chip and with package and board RLC components [11,12], there may be a long-term oscillation on the global power over several tens of clock cycles [13], which is considered to be the most severe issue related to power integrity. The long-term noise generally occurs when a circuit block goes to sleep, wakes up and changes the power status.

Although the global power grid has noise on it, the distributed voltage regulator will reduce the noise on the output of the regulator. Thus although a block changes its supply voltage in a short time and a long-term noise is generated, the voltage fluctuation on a block $V_{DD}$ is minimal. Moreover, it is supposed that the global power grid distributes the higher voltage than the local $V_{DD}$. Consequently, the change in current at the global grid is less than the case where the local $V_{DD}$ is directly connected to the global grid without the voltage down regulator even though the power fluctuation is the same amount. Thus the trigger for the noise on the global power grid is considered to be small. On the other hand, the local power grid which is connected to the output of the distributed regulator also has RLC components but they are small and will not generate the notorious long-term noise.

**VI. Conclusions**
A $V_{\text{DD}}$-hopping accelerator for an on-chip distributed power supply is proposed and 5ns transition time is experimentally verified for a linear regulator with the load capacitance equivalent to 25k NAND gates. This enables the performance improvement in dynamic $V_{\text{DD}}$ scaling systems by reducing steal time caused by the transition between different voltage levels. The transition time of 6ns is also shown by simulation for the case of a switching DC-DC converter. To further improve the effectiveness of the accelerator, two novel controller circuits are proposed.
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References


Contents of figures

Figure 1  Supply voltage trend.

Figure 2  Concept of distributed power supply system.

Figure 3  (a) Power supply and equivalent load diagram. (b) Desirable waveform (dotted line) and actual waveform (solid line) for V\textsubscript{DDINT}.

Figure 4  Basic concept of V\textsubscript{DD}-hopping accelerator.

Figure 5  Waveforms of quick raiser and quick dropper.

Figure 6  Definition of several values in case of quick dropper.

Figure 7  Speed improvement dependence on acceleration factor $\alpha$.

Figure 8  (a) Basic circuit of quick dropper and (b) its waveforms.

Figure 9  Conventional linear regulator with quick dropper.

Figure 10  Waveforms of quick dropper controller.

Figure 11  Simulated waveforms of linear regulator with and without quick dropper.

Figure 12  Chip microphotograph of the fabricated linear regulator.

Figure 13  Measured waveform of V\textsubscript{DDINT} for equivalent load of 25k NAND gates.

Figure 14  Buck converter with V\textsubscript{DD}-hopping accelerator.

Figure 15  Waveforms of V\textsubscript{DDINT} and inductor current I\textsubscript{L} when L\textsubscript{F}=21nH, C\textsubscript{L}=3nF.

Figure 16  Control timings of (a) V\textsubscript{DDH} to V\textsubscript{DDL} and (b) V\textsubscript{DDL} to V\textsubscript{DDH}.

Figure 17  Waveforms of (a) V\textsubscript{DDINT} and (b) I\textsubscript{L} when $\tau\textsubscript{N}=0$ns, $\tau\textsubscript{P}=0$ns.

Figure 18  Waveforms of (a) V\textsubscript{DDINT} and (b) I\textsubscript{L} when $\tau\textsubscript{N}=2$ns, $\tau\textsubscript{P}=2.2$ns.
Figure 19  (a) Measured and (b) simulated waveform of ringing by miss setting of $V_{\text{REF}}$.

Figure 20  (a) Modified controller circuit of quick dropper and (b) its waveforms.

Figure 21  Simulated waveform of $V_{\text{DDINT}}$ for the circuit of Fig.20 under the condition of Fig.19.

Figure 22  Basic concept of the self-aligned generation of timings.

Figure 23  Basic circuit of $V_{\text{DD}}$-hopping accelerator with self-aligned timing generator based on mirror delay circuit.

Figure 24  Simulated waveforms of self-aligned generation of timings.

Figure 25  Simulated waveforms for various values of load capacitance.

Figure 26  Diagrams of bonding wires and power grids for distributed power supply.
Fig. 1 Kohei Onizuka et al.

(a) Power supply circuit

(b) System-on-a-chip (SoC) and System-in-a-package (SiP) diagrams

Fig. 2 Kohei Onizuka et al.

(a) On-chip distributed power supply

(b) Voltage regulator and equivalent load circuit diagrams

Fig. 3 Kohei Onizuka et al.
Fig. 4  Kohei Onizuka et al.

Fig. 5  Kohei Onizuka et al.

Fig. 6  Kohei Onizuka et al.
\[ \beta : \text{achievement ratio} \]

\[ \beta = 0.9 \]

\[ \beta = 0.95 \]

\[ \beta : \text{achievement ratio} \]

Fig. 7  Kohei Onizuka et al.

Fig. 8  Kohei Onizuka et al.

Fig. 9  Kohei Onizuka et al.
Fig. 10 Kohei Onizuka et al.

Fig. 11 Kohei Onizuka et al.
Fig. 12  Kohei Onizuka et al.

Fig. 13  Kohei Onizuka et al.
Fig. 14 Kohei Onizuka et al.

(a) Duty ratio changing

(b) Output filter

Fig. 15 Kohei Onizuka et al.

(a) Output voltage of switching transistors

(b) Gate voltage of Quick dropper
Fig. 16 Kohei Onizuka et al.

Fig. 17 Kohei Onizuka et al.

Fig. 18 Kohei Onizuka et al.
Fig. 19 Kohei Onizuka et al.

Select $V_{DDH} + V_{REF}$

Pulse Gen.1

Driver

Load

Quick dropper

Fig. 20 Kohei Onizuka et al.

Select $V_{DDH} = V_{REF}$

Node A

Node B

Node C

Node D

Fig. 21 Kohei Onizuka et al.
\[ V_{DD} = \frac{V_{DDH} + V_{DDL}}{2} \]

Driver input (N1)

NMOS gate (N2)

\[ \tau_{ON}, \tau_{OFF} \]

Load

Linear regulator

Comp1

Comp2

Select \( V_{DDL} \)

N1

N2

Driver

\( \tau_{ON}, \tau_{OFF} \)

Load

Fig. 22 Kohei Onizuka et al.

Fig. 23 Kohei Onizuka et al.
Fig. 24 Kohei Onizuka et al.

Fig. 25 Kohei Onizuka et al.

Fig. 26 Kohei Onizuka et al.