A 1-ps resolution on-chip sampling oscilloscope with 64:1 tunable sampling range based on ramp waveform division scheme

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Abstract

An on-chip sampling oscilloscope with 1ps timing resolution is realized in 90nm CMOS process based on a proposed ramp waveform division scheme for precise signal integrity and power-line integrity measurement. The resolution in time is variable from 1ps to 64ps in 64 steps. A novel on-chip inductance measurement procedure is also proposed.

Keywords: sampling oscilloscope, signal integrity

Introduction

Recently power and signal integrity issues such as IR drop, di/dt noise, substrate noise, and crosstalk between interconnects are getting severer and hinders high-speed operation of VLSI's. In order to maintain the signal/power/substrate integrity, noise waveform measurement is essential but measuring the waveform on the lower-level interconnects from the outside of the chip [1] is difficult due to the higher-level metals that block the access to the lower-level metals physically and electrically. Measuring the interconnect voltage precisely from the back of the substrate is also impossible. Thus, an on-chip high-resolution oscilloscope is required. The on-chip oscilloscope should have a wide range of time resolution tenability, since the noise on a chip contains multiple frequency components caused by clocking, RLC resonance of interconnects, bonding wires, package and circuit board effects.

The fastest on-chip sampling oscilloscope ever reported achieved 100 GS/s based on a phase interpolator for the high-resolution sampling timing generation [2]. The phase interpolator circuit, however, fails to generate equally divided timing signals between two delayed signals if the delay is getting longer. Consequently, the tunable resolution range is limited to almost 2:1 and is not suitable for measuring various noise components. In this paper, a ramp waveform division scheme is proposed to achieve 1ps resolution while realizing the tunable resolution range of 64:1.

Sampling oscilloscope circuits

Fig. 1 shows a block diagram of the proposed sampling oscilloscope, which consists of one timing generator block and multiple sampling heads. The sampling oscilloscope block generates excitation timing, sampling enable timing (SE) and reference voltage (V_{REF}), which are connected to each sampling head. All timings are generated from a master clock (CK). There is no clock jitter issue nor jitter accumulation issue because all circuit operations are reset and restarted with every master clock edge. A repetitive waveform (V_{DUT}) is incident to the sampling comparator. V_{DUT} is compared with the V_{REF} at SE edge. By scanning V_{REF} and SE and monitoring '1' and '0' of the CompOUT which is a digital signal, V_{DUT} can be reconstructed. As shown in Fig.2, random noise, if there is any, can be reduced by averaging several reconstructed waveforms.

Although DUT is driven by an excitation circuit in Fig.1, excitation circuit is eliminated if noise on a chip is to be measured. In that case, CK is generated from the main clock of the circuit block under test. 128 levels of V_{REF} are generated by a resistor ladder to achieve 10mV voltage resolution. The offset voltage of the sampling comparator can be fully compensated by measuring a known DC voltage and observing the difference between the known voltage and the measured voltage. The rising edge rate of the $V_{S\&H}$ and dynamic characteristics of $M_{S\&H}$ determine the maximum measurable frequency within 10% voltage error, which is more than 20GHz estimated from the measured and simulated waveforms by applying known sinusoidal wave from outside.

Fig.3 shows a sampling timing generator based on ramp waveform division (RWD) scheme. A variable edge-rate ramp waveform is generated by a ramp generator shown in the upper half of the figure, which is compared with the static voltage, V_{SCAN}, and generates Sampling Enable (SE) signal. 64 levels of voltages in the range of $V_{SCAN,L}$ to $V_{SCAN,H}$ are generated by a resistor ladder and digitally selected step by step to generate V_{SCAN}. By scanning V_{SCAN}, the timing edge of SE is varied step by step by the minimum resolution of 1ps. The sampling time resolution can be easily varied by changing the number of I_{SRC}'s connected to V_{RAMP} smoothly up to 64ps (= 64 x 1ps). The timing resolution is measured by observing a waveform of a reference ring oscillator whose frequency is divided and monitored outside of the chip.

This oscilloscope is applied to extract inductance (L) and resistance (R) values of an on-chip line based on a novel principle. A previous approach extracts only characteristic impedance [3]. As shown in Fig.4, DUT is precharged first and then excited by a short pulse of the duration about 50ps (1). The negative voltage edge generated by the pulse travels through the line and reflected at the far-end of DUT which is open (2). The wave is reflected again at the near-end (3) and the process repeats. The waveform at the near-end of the DUT oscillates with a cycle time of $4\sqrt{LC}$ and an attenuation rate of $\exp\left(-2R\sqrt{C/L}\right)$. It is to be noted that the total charge on the DUT is decreased by the short pulse but remains unchanged during the oscillation. Since the extraction procedure employs only the cycle time and the voltage ratio information, the results do not depend on the absolute voltage value of the waveform. The measurement was carried out on a 12μm-wide and 3.8mm-long Cu line representing a power line. The extracted L and R are 0.74nH/mm and 8.0Ω/mm.

Fig.5 shows measured and simulated waveforms of a line with changing the location of a capacitor of 1.9pF representing a decoupling capacitor at the far-end, center and near-end. Good agreement is observed. The measurement is carried out at 1ps resolution and the SPICE simulation was conducted using L and R values extracted by using SPICElink field solver. A sequence of measurements for the same DUT is conducted by changing the time resolution. The measured waveforms are shown in Fig.6 to show wide tunable range of sampling resolution.

Fig.7 shows a microphotograph of a test chip fabricated in 90nm CMOS technology with a typical voltage of 1V. The test chip contains one sampling oscilloscope block and 36 DUT's for characterizing on-chip interconnects and noise. The oscilloscope uses several static analog voltages, whose lines are protected from noise sources by surrounding shield lines. The area of the each sampling head is 64µm x 35µm, while that of the sampling oscilloscope block is 0.14mm^2.

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References

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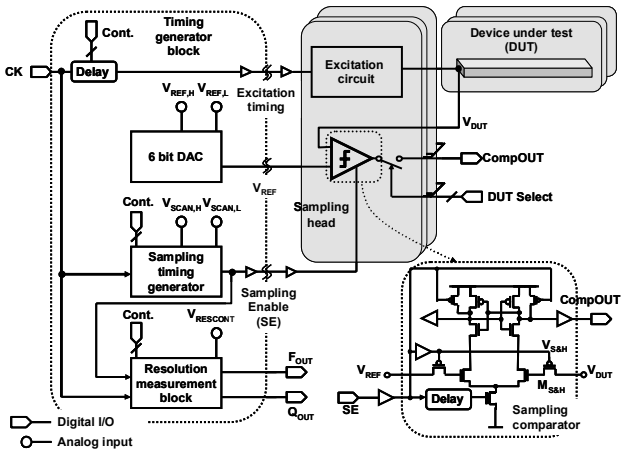

Fig.1 Overall block diagram of on-chip sampling oscilloscope

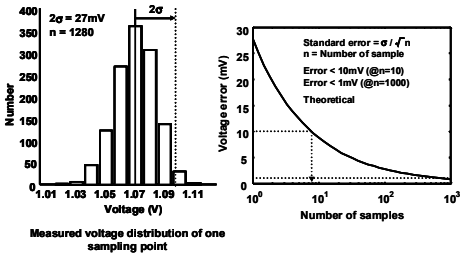

Fig.2 Measured distribution fits well with normal distribution

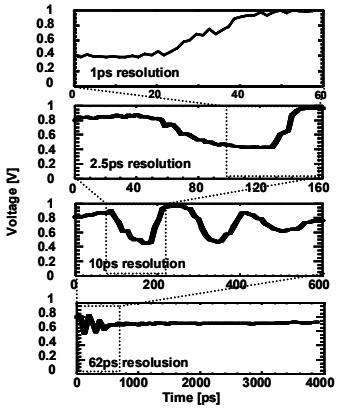

Fig.6 Same waveform measured by various timing resolutions

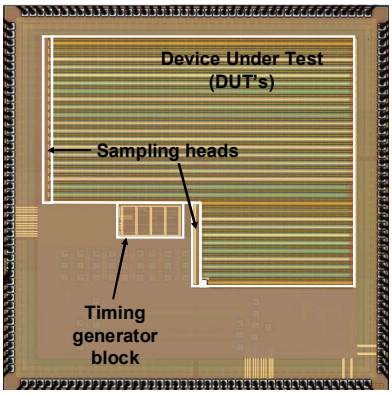

Fig.7 Photomicrograph of test chip

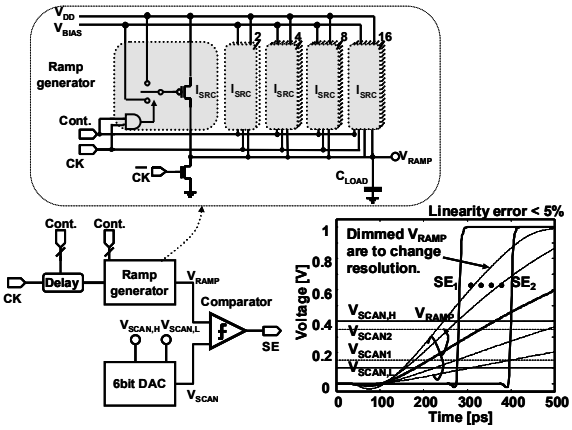

Fig.3 Ramp waveform division scheme

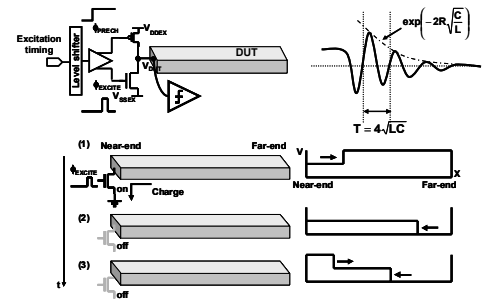

Fig.4 Measuring method of inductance and resistance

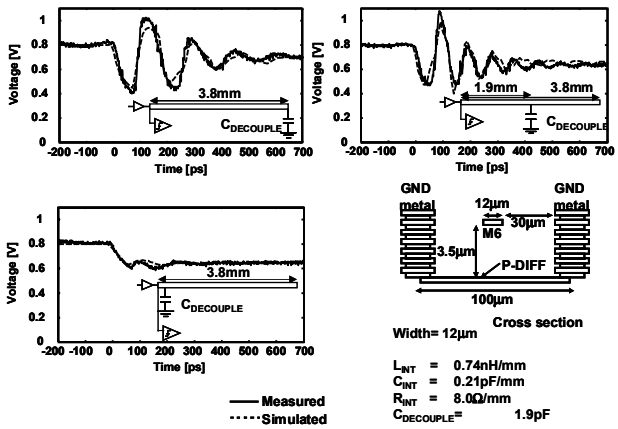

Fig.5 Measured and simulated waveforms of power supply line with varying decoupling capacitor location