Daisy Chain for Power Reduction in Inductive-Coupling CMOS Link

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Abstract

This paper discusses a daisy chain of current-drive transmitters in inductive-coupling CMOS links. Current is reused by multiple transmitters. 8 transceivers are arranged with a pitch of 20μm in 0.18μm CMOS. Transmit power is saved by 35% without sacrificing data rate (1Gb/s/ch) and BER ($<10^{-12}$) by having 4 transmitters daisy chained.

Introduction

A 1Tb/s inter-chip transceiver is developed by arranging 1024 data transceivers with a pitch of 30μm [1]. The data transceiver transmits data by inductive coupling at a data rate of 1Gb/s and consumes 3mW per channel. 70% of the power is consumed by an H-bridge circuit that controls current (I_T) through an inductor in a transmitter (Fig. 1(a)). By daisy chaining the transmitters, the current is reused by multiple channels to reduce power dissipation.

Daisy Chain Scheme

Two schemes are proposed; a Type-V scheme depicted in Fig. 1(b) (vertical concatenation) and a Type-H scheme in Fig.1(c) (horizontal concatenation). In the Type-V scheme I_T flow is controlled by turning on two transmission gates in each transmitter. Since current is reused by all the transmitters, power dissipation is reduced to $1/n$ where n is number of stages (Fig. 2).

Current flow control in the Type-H scheme is illustrated on the left of Fig. 2. When 2bit data sequence is '01', an NMOS placed in-between the two transmitters is turned on and I_T flows out to the ground. The NMOS is therefore controlled by $\overline{Txdata_0} \wedge Txdata_1$ as shown in control circuits in Fig. 1(c). When the data sequence is '10', a PMOS is turned on and I_T flows in from V_{DD}. In other cases ('00' and '11'), neither NMOS nor PMOS is turned on, and I_T flows through two transmitters to save power dissipation by 1/2. In this way, power dissipation depends on data bit sequence. Power reduction effect is calculated by generating random bit sequences and computing the power reduction effect (Fig. 2). The smaller transitions in a bit sequence, the smaller power dissipation. There is a coding method to reduce transitions in a bit sequence. MSB + xoring two consecutive bits + "1" at the end [2] may reduce transitions, and thus power dissipation as shown by a dotted line in Fig. 2. Power reduction is less than the Type-V scheme anyhow.

The Type-H scheme, however, enables higher frequency operation than the Type-V scheme, as shown in SPICE simulation results in Fig. 3. In the Type-V scheme, parasitic R and C associated with the two transmission gates in each stage degrades pulse-shaped I_T waveforms significantly as n increases. On the other hand, in the Type-H scheme, only a PMOS and an NMOS are inserted in the current pass. The current waveforms are gradually degraded only by parasitic R and C associated with the transmitter inductances. For 1Gb/s operation where 250ps width pulse with 1GHz main spectrum is used, the Type-H scheme is desirable.

Due to the RC delay associated with the transmitter inductances, data skew is caused as shown in SPICE simulation results in Fig.4. As a result, receiver timing margin is narrowed and BER is degraded. The number of stages in the Type-H daisy chain should be found experimentally by taking the power reduction effect and BER into consideration.

Testchip Design and Measurement Setup

A test chip is designed and fabricated in a 0.18μm CMOS technology. It consists of 4 types of 8-channel transmitters with different configurations as shown in Fig. 5. The transmitters are arranged with a pitch of 20μm.

Fig.6 shows a measurement setup. Two chips are mounted on two boards that are placed face to face in distance of 1-5μm. Communication distance is changed by a micromanipulator with accuracy of 1μm. Chip alignment is adjusted by using alignment marks and infrared light.

Experimental Results

Measured BER dependence on number of stages (n) is shown in Fig. 7. BER of less than 10^{-12} is verified for $n \leq 4$, while in $n=8$ BER is degraded due to the data skew.

Fig.8 shows measured BER dependence on transmit power per channel. Power dissipation is reduced by 0.7mW/ch (20%) in the 2-stage daisy chain and 1.3mW/ch (35%) in the 4-stage daisy chain without degrading data rate (1Gb/s/ch) and BER($<10^{-12}$). This result agrees with the theoretical calculation in Fig.2.

Conclusions

Two daisy chain schemes are proposed and investigated. The Type-H daisy chain of 4 transmitters saves transmit power by 35% without sacrificing data rate (1Gb/s/ch) and BER ($<10^{-12}$).

Acknowledgements

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References

[1] N. Miura, *et al*., "A 1Tb/s 3W Inductive-Coupling Transceiver for Inter-Chip Clock and Data Link," to be published in *ISSCC Digest of Tecnical. Papers*, Feb. 2006.

[2] Youngsoo Shin, private communication, 2006.

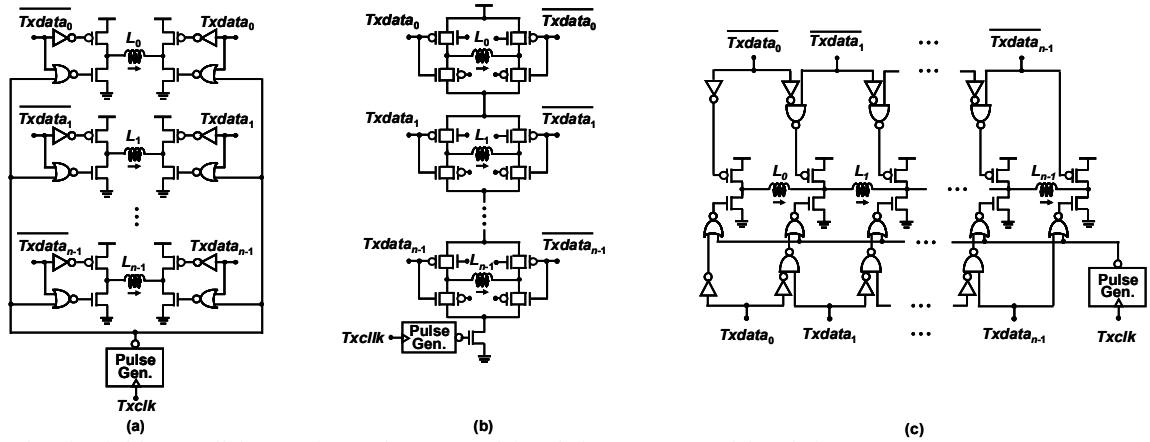

Fig.1 (a) Conventional H-bridge parallel transmitters, (b) Type-V daisy chain, (c) Type-H daisy chain.

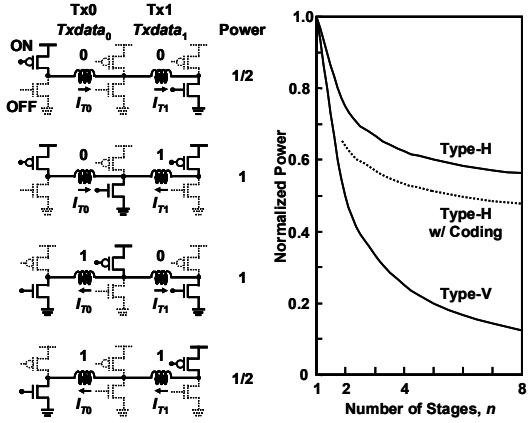

Fig.2 Calculated power reduction.

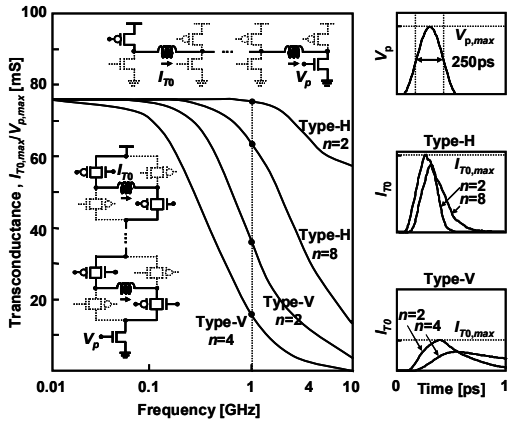

Fig.3 Simulated frequency characteristics of transconductance.

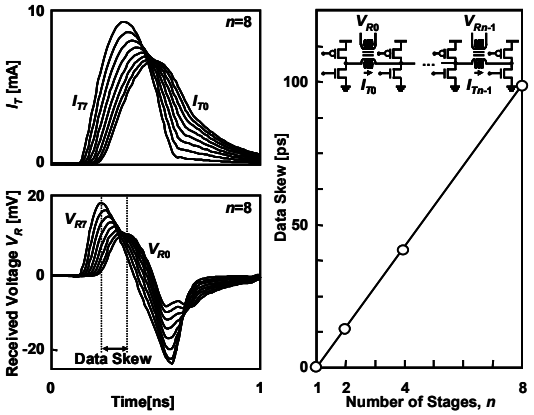

Fig.4 Simulated data skew dependence on number of stages.

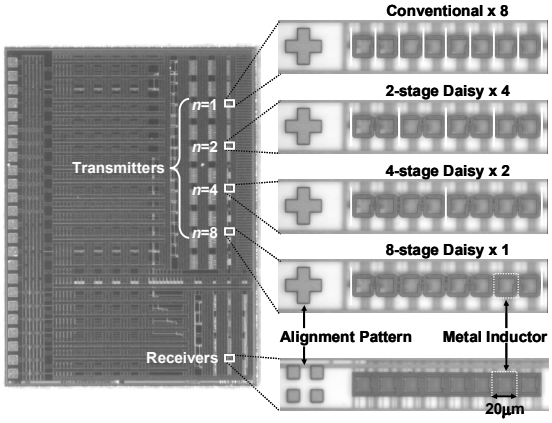

Fig.5 Chip microphotograph.

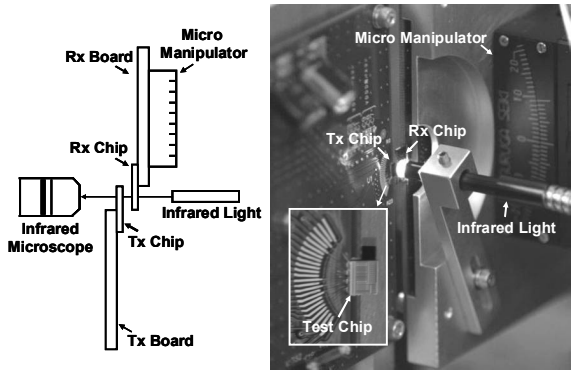

Fig.6 Experimental setup.

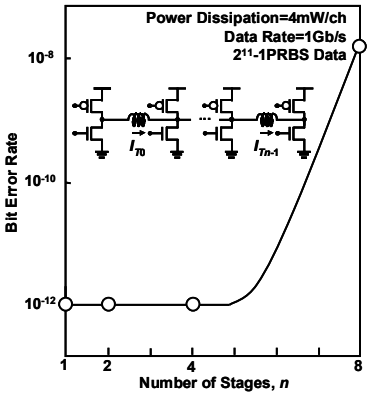

Fig.7 Measured BER dependence on number of stages.

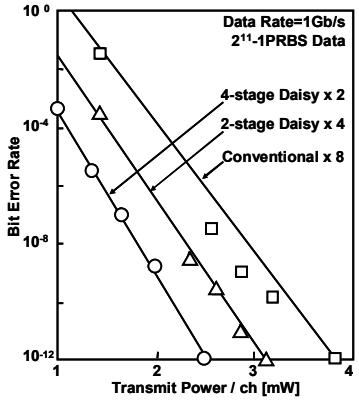

Fig.8 Measured BER dependence on transmit power.