# Suppression of DC bias stress-induced degradation of organic field-effect transistors using postannealing effects

Tsuyoshi Sekitani, Shingo Iba, Yusaku Kato, Yoshiaki Noguchi, and Takao Someya[a)]
*Quantum-Phase Electronics Center, School of Engineering, The University of Tokyo, 7-3-1 Hongo, Bunkyo-ku, Tokyo 113-8656, Japan*

Takayasu Sakurai
*Center for Collaborative Research, The University of Tokyo, 4-6-1 Komaba, Meguro-ku, Tokyo 153-8505, Japan*

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We fabricate pentacene field-effect transistors (FETs) showing a very small degradation in performance under a continuous DC bias stress. Pentacene FETs are manufactured on polyimide films with polyimide gate dielectric layers, and then encapsulated by poly-chloro-para-xylylene passivation layers, resulting in very flexible and heat-resistant devices. When such devices are annealed at 140 °C for 12 h in a nitrogen environment, the change in their source-drain current is $3\pm1\%$ even after the application of continuous DC voltage biases of $V_{DS}=V_{GS}=-40$ V for 11 h. Furthermore, their mobility is increased by postannealing effects from 0.27 $cm^2/V\,s$ to 0.36 $cm^2/V\,s$ and their on/off ratio is also increased from $10^3$ to $10^6$. © *2005 American Institute of Physics*. [DOI: 10.1063/1.2031932]

Organic field-effect transistors (FETs) have been recognized as one of key technologies for realizing flexible, lightweight, printable, and large-area electronics. Owing to the extensive effort to improve the fabrication and construction materials of organic semiconductors, gate dielectrics, and electrodes, electric circuits consisting of organic transistors have been manufactured for applications in driving devices for paper like displays,[1,2] radio-frequency identification tags,[3,4] and large-area sensors.[5,6] To realize such applications, one of the important issues is the reliability and stability of organic transistors. Many degradation processes of organic transistors are induced by oxygen-and moisture-associated species and can thus be minimized by adequate encapsulation. However, other problems exist, such as drifts in transistor performance with DC bias stress application, namely, current degradation associated with threshold voltage ($V_{th}$) drift, hereafter referred to as DC bias stress effects.[7–9] Such drifts have also been observed in amorphous- and polycrystalline-silicon-based transistors,[10–13] which are understood to originate from the deep trapping of conduction carriers. The suppression of DC bias stress effects is crucial to the reliable driving of sophisticated organic integrated circuits.

In this work, we manufactured pentacene FETs on polyimide base films with polyimide gate dielectric layers that were encapsulated by poly-chloro-para-xylylene passivation layers and annealed at 140 °C for 12 h in a nitrogen environment. We suppressed the degradation in the transistor's performance induced by the application of a continuous DC bias stress. After the postannealing of the FETs, their mobility increased from 0.27 $cm^2/V\,s$ to 0.36 $cm^2/V\,s$, and their on/off ratio increased from $2.4\times10^3$ to $2.5\times10^6$, at which $V_{th}$ shifted from −4 V to −6 V. The annealed FETs showed no significant changes in performance even after the application of continuous DC voltage biases of $V_{DS}=V_{GS}=-40$ V for 11 h, namely, the degradations in source-drain current associated with the DC bias stress-induced drift in $V_{th}$ was suppressed within $3\pm1\%$.

Pentacene FETs, the cross-sectional illustration of which is shown in Fig. 1(a), were fabricated on plastic films without using an *in situ* procedure. A gate electrode (G) consisting of a 5-nm-thick Cr layer (adhesion layer) and a 100-nm-thick Au layer was deposited through a shadow mask in a vacuum evaporator on a 75-$\mu$m-thick polyimide film. Then, polyimide precursors (KEMITITE CT4112, Kyocera Chemical Co., Ltd.) were spin-coated and cured at 180 °C for 1 h to form 600-nm-thick gate dielectric layers.[5,6,14] A 50-nm-thick pentacene layer was deposited in the vacuum evaporator as a channel, and then 50-nm-thick Au drain (D) and source electrodes (S) were evaporated through a shadow mask. The channel length (L) and width (W) of the pentacene FETs were 100 $\mu$m and 1 mm, respectively. Then, the base film with transistors was uniformly encapsulated with a 6-$\mu$m-thick poly-chloro-para-xylylene (dix-SR, Daisankasei Co., Ltd.) passivation layer, hereafter referred to as a parylene layer.[15] For electronic interconnections, a $CO_2$ laser drill was used to make via holes through the parylene passivation layer on the source and drain elec-

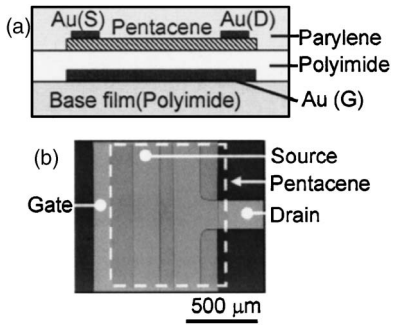


FIG. 1. (a) The cross sectional illustration of an organic transistor on a polyimide base film with a polyimide gate dielectric layer and a parylene passivation layer. (b) A micrograph of the manufactured FET. The dashed-line represents the area of pentacene.

[a)]Author to whom correspondence should be addressed; electronic mail: someya@ap.t.u-tokyo.ac.jp

 

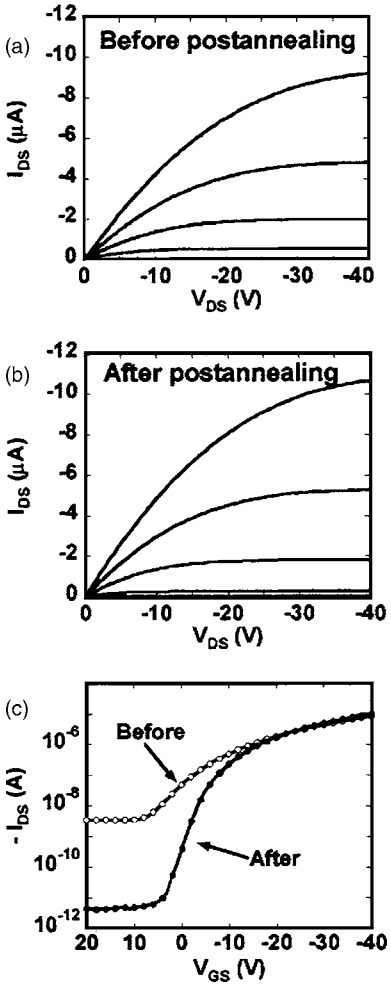


FIG. 2. Typical DC characteristics of present FETs before and after postannealing Source-drain current ($I_{DS}$) is measured in an ambient environment as a function of source-drain voltage ($V_{DS}$) (a) before and (b) after postannealing. Gate voltage ($V_{GS}$) is changed from 0 to −40 V in −10 V steps. (c) Corresponding transfer curves taken before and after postannealing: $V_{GS}$ is swept from +20 to −40 V with the application of $V_{DS}$=−40 V.

trodes and through the polyimide layer on the gate electrode. Then Au pads were deposited to connect all the electrodes through via holes. Finally, the encapsulated FETs were annealed at 140 °C for 12 h in a nitrogen environment, hereafter referred to as the postannealing. Figure 1(b) shows a micrograph of the manufactured device. A parylene layer has a high heat resistance and an excellent functionality as a passivation layer, which prevents organic semiconductors from degradations associated with direct exposure to ambient air.

The typical current-voltage characteristics of the FETs were measured with a precision semiconductor parameter analyzer (4156C, Agilent Technologies) and a probe station in a light-shielded ambient environment. Figure 2 shows the typical DC characteristics of the FETs at room temperature. We monitored the source-drain current ($I_{DS}$) of the FETs as a function of source-drain voltage ($V_{DS}$), as shown in Figs. 2(a) and 2(b), which are taken before and after the postannealing of the same device, respectively. Gate voltage ($V_{GS}$) was changed from 0 V to −40 V in −10 V steps. Figure 2(c) shows corresponding transfer curves of the device before and after the postannealing. $V_{GS}$ was swept from +20 V to −40 V with the application of $V_{DS}$=−40 V. Mobility was

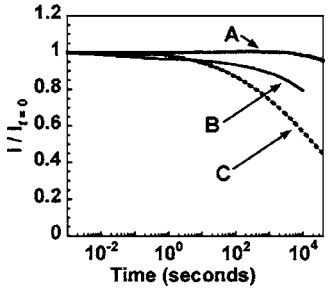


FIG. 3. Normalized source-drain current ($I_{DS}$) under continuous DC voltage biases ($V_{GS}$=$V_{DS}$=−40 V) as function of time $t$. $I_{t=0}$ represents $I_{DS}$ at the start of the measurement ($t$=0). Measurements are performed on (A) the annealed and (B) nonannealed FETs on polyimide base films with polyimide gate dielectric layers (solid line), and on (C) nonannealed FETs on Si substrates with $SiO_2$ gate dielectric layers (dashed line), for comparison.

increased from 0.27 $cm^2/V\,s$ to 0.36 $cm^2/V\,s$ when we evaluated the mobility in the saturation regime after the postannealing. Subthreshold swing decreased from 7 V/decade to 2 V/decade, indicating improved characteristics of the annealed FETs. Furthermore, off-state currents decreased by three orders of magnitude after the postannealing,[16] although on-state current increased from −8.5 μA to −10.5 μA. As a result, the maximum on/off current ratio markedly increased from $2.4\times10^3$ to $2.5\times10^6$ when this parameter was evaluated before and after the postannealing.

During the postannealing for 12 h, $V_{th}$ systematically increased from −4 V to −6 V. As a result, on/off ratio also increased from $10^2$ to $10^6$ with off-state current defined at $V_{GS}$=0 V, which is crucial to the low power dissipation of circuits.

We measured the source-drain current ($I_{DS}$) of the FETs before and after the postannealing under continuous DC voltage biases of $V_{GS}$=$V_{DS}$=−40 V. The measurements were performed in a light-shielded globe box with oxygen and moisture each at less than 1 ppm to exclude other extrinsic effects that are not associated with DC bias stress for many hours, since organic transistors are sensitive to ambient conditions, such as light, temperature, and atmospheric air. Figure 3 shows $I_{DS}$ normalized by the data at the start of the measurement ($t$=0) as a function of time $t$. Even after the application of continuous voltage biases of $V_{GS}$=$V_{DS}$=−40 V for 11 h, the decrease in $I_{DS}$ is 3±1% for the annealed FETs, as denoted by (A) in Fig. 3, while that for the nonannealed FETs is large at more than 20%. Similar measurements were also performed on the nonannealed pentacene FETs prepared on Si substrates with $SiO_2$ gate dielectric layers, for comparison, where structural parameters except Si and $SiO_2$ layers are identical. In Fig. 3, the nonannealed pentacene FETs on $SiO_2$ gate dielectric layers show a larger degradation than the annealed and nonannealed FETs with polyimide gate dielectric layers, clearly indicating that deep trapping sites are distributed at the interface associated with $SiO_2$ as well as with polyimide gate dielectric layers.

We also investigated the performance of the FETs after the application of a continuous DC bias stress. After the application of DC bias stress for 11 hours, the annealed FETs showed a very small change in saturation current from −10.5 μA to −10.1 μA, at which the mobility and maximum on/off ratio were evaluated to be 0.36 $cm^2/V\,s$ and $2.5\times10^6$, respectively. The threshold voltage shift was less

than 0.4 V, indicating almost no DC bias stress-induced degradations of the annealed FETs. Such negligible degradations in $I_{DS}$ and $V_{th}$ drift have not yet been achieved in organic transistors thus far.[7–9] In amorphous- and polycrystalline-silicon-based transistors, the changes in $V_{th}$ and $I_{DS}$ associated with DC bias stress can be understood well by the qualitative analysis of the deep trapping of conduction carriers,[10–13] where major progress has been made to suppress the degradations by the surface modification of gate dielectric layers,[12] chemical doping of semiconductors, biases application to substrates, and device annealing for eliminating vacancies and/or lattice defects as candidate deep-trapping potential sites.[13,17] Control techniques for $V_{th}$ and $I_{DS}$ in silicon based FETs are convenient and efficient. In contrast, the accurate surface modification of polymer gate dielectric layers and chemical doping of organic semiconductors are far more complex technologies due to the unreliability of manufacturing process and/or performance of organic transistors. The application of bias from substrates is not practical for organic transistors because these devices are usually fabricated on nonconductive plastic substrates for flexibility. Therefore, we should employ postannealing in organic transistors. Vacancies and/or lattice defects in organic materials are easy to eliminate by annealing. Furthermore, annealing leads to more ordering and/or optimal structures of pentacene and polyimide molecules, and better matching at the interface, resulting in higher mobilities at room temperature. Molecular ordering, the elimination of vacancies and molecular defects, and recrystallization by annealing have often been clearly observed in many organic materials including pentacene and polyimide.[18–21]

It is very interesting to note in the present postannealing that, even though the annealed FETs were exposed to ambient air after the postannealing in a nitrogen environment, the characteristics of the annealed FETs did not deteriorate owing to the parylene passivation layers. This result suggests that postannealing effects are conveniently irreversible, thus complex *in situ* procedures can be excluded from the fabrication of such FETs. It is crucial to realize more sophisticated organic ICs because a large on/off ratio should result in a low power dissipation of circuits.

Since many organic materials have low heat-resistances and large thermal expansion coefficients, the high-temperature postannealing of organic FETs usually results in device failures associated with the decomposition of organic materials and/or thermal stress at the interface between layers. However, in this work, we employed high heat-resistant polyimide for the gate dielectric layers and base films. Polyimide gate dielectric layers have a perfect matching of the thermal expansion coefficient with polyimide base films, leading to a reduction in thermal stress. Such an excellent thermal stability of the present organic FETs leads to the realization of effective postannealing effects at high temperatures.

In summary, we have suppressed the DC bias stress-induced degradation in the performance of organic FETs using encapsulation and high temperature postannealing effects. The stability of the FETs' characteristics, such as mobility, $V_{th}$, and $I_{DS}$, under a continuous DC bias stress enables us to realize reliable and sophisticated integrated circuits consisting of organic transistors.

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