V_{DD}-Hopping Accelerator for On-Chip Power Supplies Achieving Nano-Second Order Transient Time

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***Abstract*— A V_{DD}-hopping accelerator for on-chip power supply circuits is proposed and the effectiveness of the accelerator circuit is experimentally verified. The circuit enables nano-second order transient time in on-chip distributed power supply systems. The measured transition time is less than 5ns with load circuit equivalent to 25k logic gates in 0.18-µm CMOS. This is to be compared with the case without the accelerator of the order of µs and thus the acceleration by two orders of magnitude is achieved. Automatic generation of the timings in a self-aligned manner is also discussed.**

I. INTRODUCTION

System-on-a-Chip (SoC) and System-in-a-Package (SiP) have become major integration technologies in recent years. They are often used for integrating various types of circuit blocks like MPU, DRAM, ROM, logic and analog circuits on a chip or in a package. The optimum supply voltages (V_{DD}) for these types of circuit blocks differ among themselves and the difference tends to increase as the technology scales. This leads to the multiple-V_{DD} implementation in low-power and high-performance systems. Supplying many different voltages from outside the package gives rise to much overhead in area and the power line integrity including IR drop and noise also becomes an issue.

The distributed on-chip power supply circuits are useful for solving these problems. Fig.1 shows the concept of the distributed power supply. On-chip power supplies on each chip/circuit block convert the external V_{DD} into the optimized internal V_{DD} of the target block.

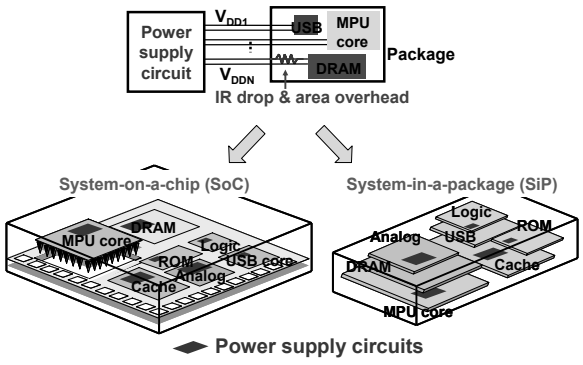

Figure 1. Concept of distributed power supply system.

For each block, the highest speed is not always required for all the time. It has been known that changing V_{DD} depending on the required speed reduces power consumption. Especially, a discrete version of V_{DD} scaling approach, namely, V_{DD}-hopping where V_{DD} is scaled adaptive to the required performance was shown to be effective in reducing power consumption while maintaining real-time feature in multimedia systems [1][2]. From a view point of the commercialization, however, it is impractical to test and verify all circuit blocks in continuous range of V_{DD}. It means that circuits are allowed to operate only at discrete levels of V_{DD}, that is, the circuit operation has to be stopped during V_{DD} transition from one level to another. Therefore, high-speed V_{DD}-hopping is important not to steal much time for the voltage hopping from the normal operation.

From the power supply circuit, CMOS circuits including logic, memory and analog blocks are approximated as R and C as is shown in Fig.2. Fig.2(a) shows the diagram of an on-chip power supply and an equivalent load circuit. C_L represents to MOSFET capacitances, interconnection capacitances and decoupling capacitances and R_L relates to the power consumption of the load circuit. When a load circuit is stopped, the circuit draws only leakage current and R_L increases up to mega-ohm range. Thus, in the transient period of the VDD-hopping process when the load circuit stops operation, there is eventually no path to pull down the internal voltage to the lower level and the transient becomes extremely long. Fig.2(b) shows an example of an ideal

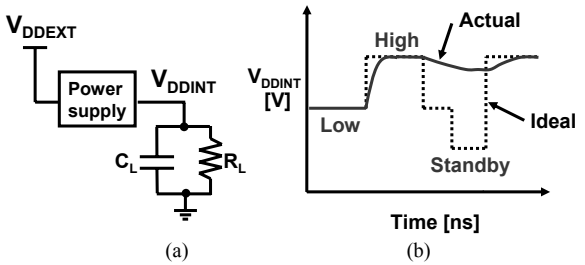

Figure 2. (a) Power supply and equivalent load diagram. (b) Desireable waveform (dotted line) and actual waveform (solid line) for V_{DDINT}.

waveform for the internal V_{DD} (V_{DDINT}) and the actual waveform. The inductive effects of V_{DDINT} lines can be neglected, since the power line length is short in case of on-chip power supplies. The long transition time steals much time in the V_{DD}-hopping and reduces performance of the system. Therefore, techniques to reduce the transition time are needed.

II. Basic Concept of V_{DD}-Hopping Accelerator

Fig.3 shows the basic concept of the V_{DD}-hopping accelerator. The NMOS transistor labeled "quick dropper" accelerates the discharging process.

The basic circuit and waveforms of the quick dropper are shown in Figs.4 and 5. The transition time depends on the RC time constant of C_L and the effective resistance of the quick dropper, R_{ON}. Since the quick dropper discharges C_L not aiming at V_{DDL} but aiming at much lower voltage of V_{SS}, the discharging time is more highly accelerated.

The quick dropper must be turned off slightly earlier before the V_{DDINT} reaches the final voltage of V_{DDL} because there is delay τ_{OFF}, in switching off the dropper. In order to take this delay into account, V_{REF} which sets the voltage at which the driver for the dropper starts the turning-off process should be a little higher than V_{DDL} as follows.

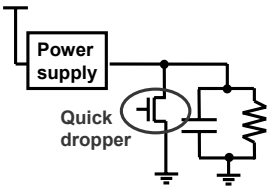

Figure 3. Basic concept of V_{DD}-hopping accelerator.

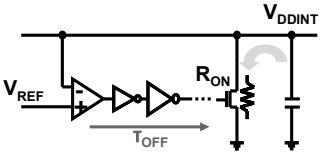

Figure 4. Basic circuit of quick dropper.

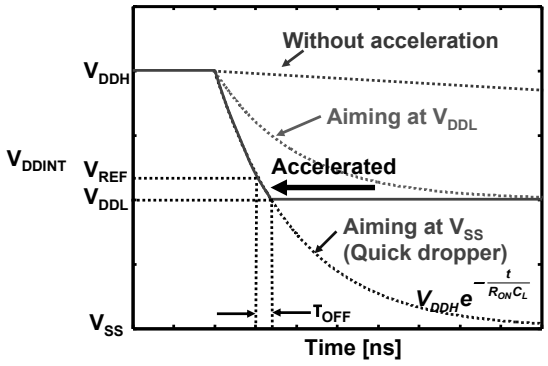

Figure 5. Waveforms of quick dropper.

$$V_{REF} = V_{DDL} e^{\frac{\tau_{OFF}}{R_{ON} C_L}}. \qquad (1)$$

V_{REF} is supplied from external to the chip for the measurement but self-aligned generation of the timing is also discussed later in this paper. Lines to distribute V_{REF} do not give much overhead in area because there is no need to draw current through the line.

III. Implementations

Implementations of the V_{DD}-hopping accelerator for several types of power supply are presented in this section. Circuit diagrams of the quick dropper for linear regulator, buck converter and switched capacitor converter are shown in Figs.6,7 and 8 respectively.

Fig.9 shows the waveforms for the quick dropper. τ_{ON} and τ_{OFF} signify the delay of the quick dropper driver to turn on and turn off the dropper itself, respectively. To avoid the output voltage ripple like a voltage overshoot and undershoot,

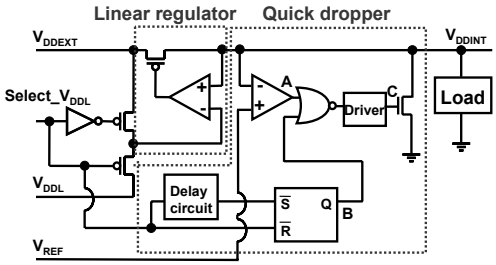

Figure 6. Linear regulator with quick dropper.

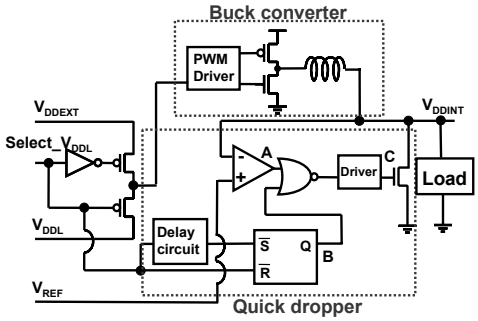

Figure 7. Buck converter with quick dropper.

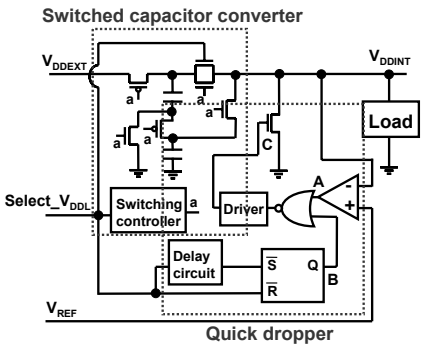

Figure 8. Switched capacitor converter with quick dropper.

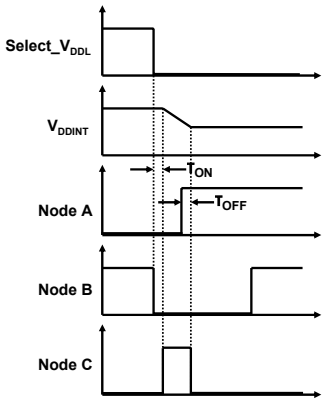

Figure 9. Waveforms of quick dropper.

an accurate setting of V_{REF} is needed.

IV. SIMULATION AND MEASUREMENT RESULTS

To verify the effectiveness of V_{DD}-hopping accelerator, the quick dropper for the linear regulator shown in Fig.6 was designed in 0.18-µm CMOS. The load circuit is designed to be equivalent to 25k NAND gates.

Fig.10 shows the simulated waveforms of the linear regulator with and without a quick dropper using HSPICE. Here, the leakage power is assumed to be 1% of the dynamic load circuit power. V_{DDH} and V_{DDL} equal to 2.0V and 1.5V respectively. The transition time is defined the time from the start of the Select_V_{DDL} to the time when the V_{DDL} trips 95% of V_{DDH}-V_{DDL}. The transition time from V_{DDH} to V_{DDL} without quick dropper is much over 50ns because the capacitance is discharged only by the leakage. It is impossible to start operation of the load circuit in the V_{DDL} term. The transition time with the quick dropper is about 3ns while that without the quick dropper is 0.4µs. The voltage ripple right after the transition is smaller than 2% and thus it is possible to start the operation of the load circuit right after the transition.

A chip microphotograph of the fabricated linear regulator with the quick dropper is shown in Fig. 11. The quick dropper area is 20x20µm, while the linear regulator area is 30x70µm. The area overhead of the quick dropper can be as small as 2% of the load circuit.

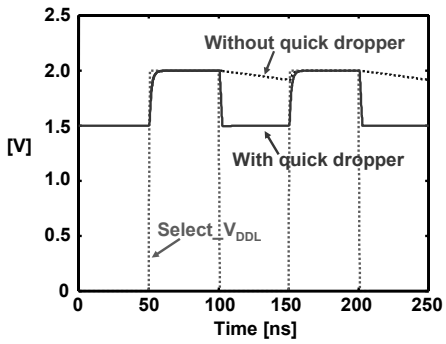

Figure 10. Simulated waveforms of the linear regulator with and without a quick dropper.

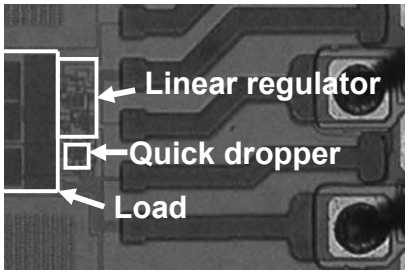

Figure 11. Chip microphotograph of the fabricated linear regulator whith the quick dropper. The size of the proposed accelerator is 35x35µm and it is seen that the accelerator is much smaller compared with a bonding pad.

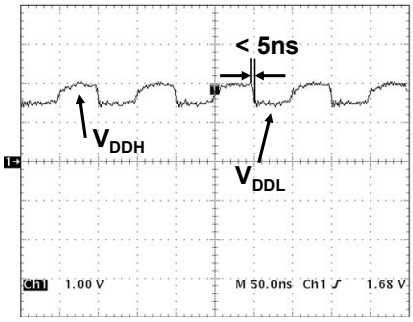

Figure 12. Measured waveform of V_{DDINT}.

Fig.12 shows the measured waveform for V_{DDINT} which coincides well with the HSPICE simulation. It is seen that the transition time from V_{DDH} to V_{DDL} is smaller than 5ns which enables more than two orders of acceleration over the case without the accelerator circuit.

V. CONTROL METHODOLOGY MODIFICATION

The generation of all the timings for the circuit described in the previous sections requires V_{REF} which is provided from outside the package. This is doable since the V_{REF} does not carry current and the area overhead is small even although the V_{REF} line is shielded from adjacent signals by using narrowest V_{SS} lines. The V_{REF} is dependent on load circuit as is expressed in (1). If all timing signals can be generated on a chip indifferent from the load circuit, the applicability of the circuit in SoC/SiP environments increases. To address this issue, automatic generation of the timings in a self-aligned manner is considered in this section.

Fig. 13 shows the concept of the proposed approach. It is possible to approximate the exponential voltage waveform by a linear transition. Therefore, once the delay required from the start of the transition to the half point of the trip to V_{DDL} is known, the remaining transition time to V_{DDL} is predictable. The half voltage can be generated by a simple on-chip circuit. V_{DDL} is to be distributed but it is the same for

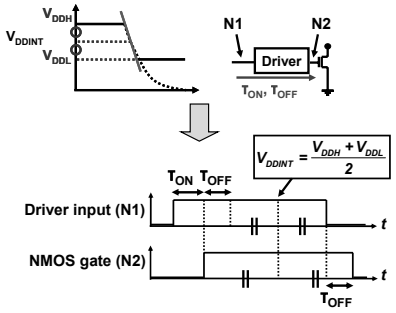

Figure 13. Basic concept of the self-aligned generation of timings.

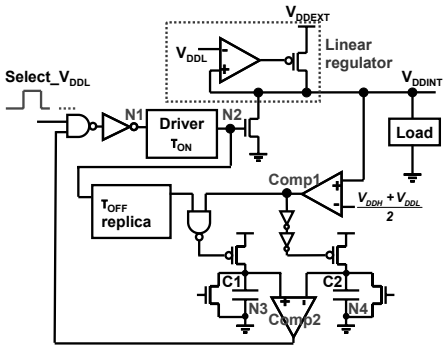

Figure 14. Basic concept of V_{DD}-hopping accelerator with self-aligned timing generator based on a mirror delay circuit.

all the circuit blocks while V_{REF} is different for each circuit blocks.

Fig. 14 shows the circuit diagram of a quick dropper with the proposed control. The timing sequence shown in Fig. 13 can be implemented by a mirror-delay circuit which consists of two capacitors C1 and C2. Fig. 15 shows the simulated waveforms of the circuit by HSPICE in 0.18-μm CMOS. Here, it is assumed that V_{DDH}=2.0V and V_{DDL}=1.2V.

The mirror-delay circuit works as follows. At the start, both of C1 and C2 are discharged to V_{SS}. Then, charging of C1 is started when the time span of $\tau_{ON}+\tau_{OFF}$ passed. The charging process ends when V_{DDINT} reaches the middle voltage of V_{DDH} and V_{DDL}. Then, charging of C2 begins. When the terminal voltage of C1 and C2 gets equal, the turn-off process for the dropper transistor is initiated. In this process, the delay adjustment for $\tau_{ON}+\tau_{OFF}$ is required to compensate the delay for the driver circuit of the dropper transistor. This can be achieved by a help of a replica circuit as shown in the figure.

Fig. 16 shows the simulated waveforms of V_{DDINT} when the load capacitance C_L varies from 15pF to 30pF. It is seen from the figure that the final voltage of V_{DDL} is achieved for a wide range of C_L without changing the control circuit itself. Thus the self-aligned feature is verified.

It is possible to widen the range of C_L furthermore by using variable capacitors for C1 and C2. The value of capacitors is fixed after the test sequence at the starting up of the load circuit.

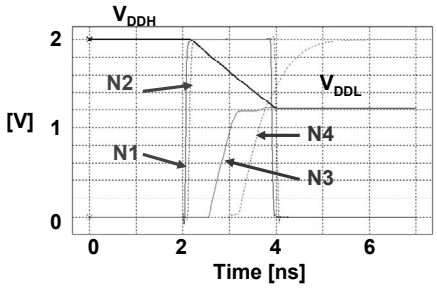

Figure 15. Simulated waveforms of the self-aligned generation of timings.

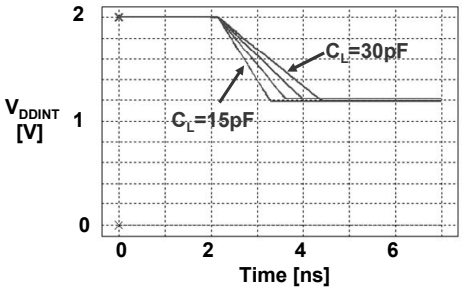

Figure 16. Simulated waveforms for various values of load capacitance.

VI. CONCLUSIONS

A V_{DD}-hopping accelerator design for on-chip distributed power supplies is presented. The measured transition time less than 5ns for a load capacitance equivalent to 25k NAND gates is achieved. This enables the performance improvement in dynamic V_{DD} scaling systems by reducing steal time caused by the transition between different voltage levels.

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