Statistical Leakage Current Reduction in High-Leakage Environments Using Locality of Block Activation in Time Domain

Jin-Hyeok Choi, *Member, IEEE*, Yingxue Xu, and Takayasu Sakurai, *Fellow, IEEE*

***Abstract*—This paper describes a new leakage current reduction methodology that can give a statistical leakage current reduction even if the chip is in active mode, as well as in sleep mode. The proposed scheme utilizes a time locality of activation probability of a given circuit block like cache memory characteristics. The leakage cut-off switch is operated by a self-timed sleep timer, which puts the block into sleep mode. By waiting for a certain number of cycles before entering sleep mode, power overhead associated with the sleep and wake-up process is optimized, and its conditional probability is also analyzed. The effectiveness of the proposed scheme is verified by an 8-bit RISC microprocessor using Verilog HDL with real firmware, and demonstrated by a 64-bit carry-look-ahead adder with the self-cut-off switch fabricated with dual-threshold voltage SOI technology. The criterion of the effectiveness of the proposed scheme is also discussed.**

***Index Terms*—Leakage current, low power, MTCMOS, standby current.**

I. Introduction

POWER considerations have become an increasingly dominant factor in the VLSI systems, especially for portable and battery-powered systems. Power consumption in digital circuits can be attributed to dynamic switching power and leakage power. Dynamic switching power is the dominant component of power consumption in modern digital integrated circuits. As semiconductor technology scales down, however, operation voltage is lowered to reduce power consumption of the circuits, and to guarantee the device reliability. In order to maintain performance, one must scale threshold voltages as well [1], which results in exponential power increase by leakage current. It is anticipated that the leakage power will become comparable to the dynamic power in the near future [2], and will become a dominant component in active power [3]. There have been many papers on reduction of leakage current during standby modes. Examples include using multithreshold voltage CMOS (MTCMOS) [4], [5] to cut the leakage current off by high-threshold voltage transistor, or utilizing reverse body bias to achieve a variable threshold voltage CMOS (VTCMOS) [6]–[8], as shown in Fig. 1. Various switch structures, such as BGMOS [9] and ZSCCMOS [10], have also been proposed and analyzed. However, those techniques are based on the fact that the standby signal is generated by an internal control circuit or by issuing command from an external host. As well as the power-aware design for the sleep mode just mentioned, an adaptive supply voltage scheme has been reported for active dynamic power reduction in [11]. However, little attention has been given to handling the leakage current in active mode.

This paper presents a new switching methodology that can give a statistical leakage current reduction to cut off the leakage current even if the chip is in active mode, as well as in sleep mode. One of the major obstacles to put a given block into sleep mode is long wake-up time. Recently, a new cut-off switching scheme, called the zigzag super cut-off scheme (ZSCCMOS), has been proposed to shorten the wake-up time by almost an order of magnitude [10], so that it can make the block usable in the next clock cycle.

The greatest issue in the leakage cut-off scheme by inserting the cut-off switch is that the sleep and the wake-up processes need dynamic power to turn on and off the cut-off switch, so that frequent sleeping and activation of a block may increase the total energy, although leakage power may be reduced. This paper shows that block activation rate has a time locality like cache memory hit characteristics, and demonstrates that the active leakage can be reduced by utilizing locality of block reactivation in time domain.

The feasibility of the proposed method is verified by an 8-bit RISC microprocessor using Verilog Hardware Description Language (HDL). It is proved that the proposed leakage reduction scheme can give leakage current reduction in active mode using block activation data of real applications and simulations. The effectiveness of the proposed scheme is also demonstrated by the leakage measurement of 64-bit carry-look-ahead adder (CLA) with self-timed cut-off switch fabricated on SOI substrate having dual threshold voltage (V_{TH}) technology.

II. Leakage Current Reduction Scheme

A. Leakage Equivalent Sleep Time

The concept of the proposed method utilizes the fact that not all the circuit blocks on a chip operate even though the chip is in active mode. For example, when a microcontroller unit (MCU) is receiving burst data of 2 kB from a host and writing them in flash memory of a mobile memory card, it takes several hundreds of microseconds to finish the task, but only direct memory

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J.-H. Choi was with the Center for Collaborative Research and Institute of Industrial Science, University of Tokyo, Tokyo 153-8505, Japan. He is now with System LSI Division, Samsung Electronics Company Ltd., Yongin-City 449-711, Korea (e-mail: jinhchoi@hanmail.net).

Y. Xu and T. Sakurai are with the Center for Collaborative Research and Institute of Industrial Science, University of Tokyo, Tokyo 153-8505, Japan (e-mail: tsakurai@iis.u-tokyo.ac.jp).

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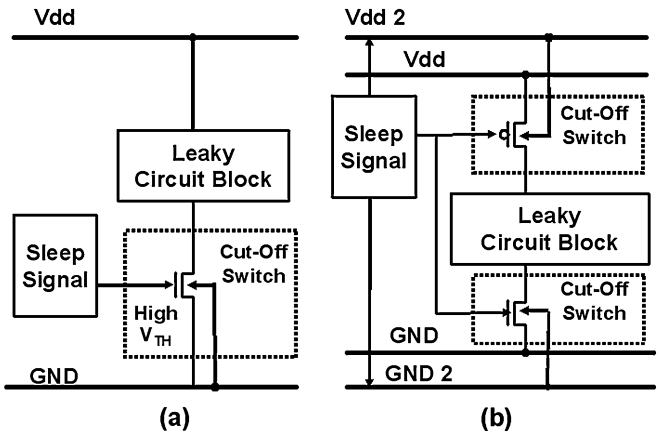


Fig. 1. Block diagrams of two cut-off schemes. (a) MTCMOS. (b) VTCMOS.

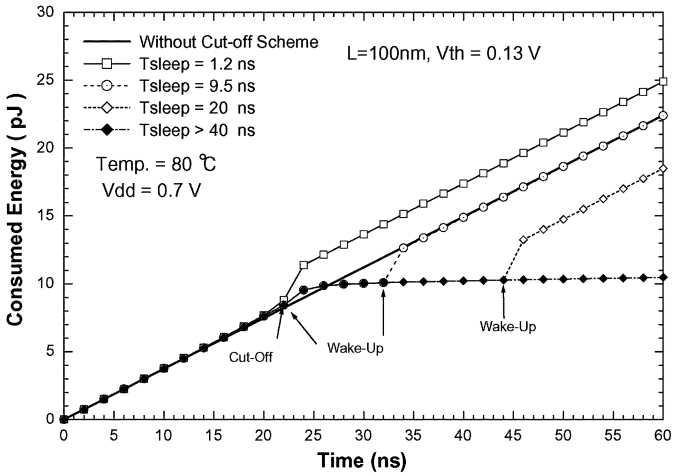


Fig. 2. Simulated results of the 64-bit carry-look-ahead adder with respect to various sleep times. It is derived from the viewpoint of $V_{\rm DD}$, so the discharge current to ground is added next recharge current.

access (DMA) and I/O-related blocks are working in data receiving and transferring. The internal CPU operates to verify the error correction code (ECC), to check the interrupt signal, and to calculate the mapping address of flash memory. The other blocks do not or rarely work, but still consume leakage current. This may be not serious so far, but will be a serious power consumption factor in the leakage dominant era.

Fig. 1 shows the block diagram of the cut-off switch scheme having MTCMOS and VTCMOS. The sleep signal should be issued from an internal control circuit or an external host to make the block sleep. Fig. 2 shows simulated energy consumption behaviors of the 64-bit carry-look-ahead adder (CLA) with various sleep duration from the viewpoint of the power node ($V_{\rm DD}$). The 100-nm MOS model parameters by Berkeley Predictive Technology Model are used with modified threshold voltage. The energy overhead associated with the sleep and wake-up process is shown in the figure. The simulated results show that the turning on/off of 1.2-ns interval causes an increase of energy consumption, while that of 20-ns interval achieves energy saving. In 9.5-ns interval, the leakage energy saved by cutting off the block is the same as the active energy consumed by the switching operation.

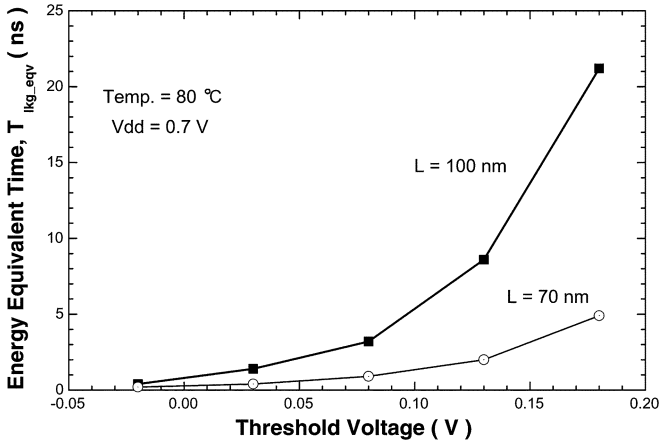


Fig. 3. Estimated leakage energy equivalent times with the variations of threshold voltage and channel length.

The energy consumption associated with turning on and off the block are expressed as $E_{\rm switch}$, which represents the operation energy of the switch driver and its control circuit. The energy saved by turning off a given block for the duration of cut-off time, $T_{\rm sleep}$, can be expressed as $(P_{\rm lkg} - P_{\rm sleep})$, where $P_{\rm lkg}$, and $P_{\rm sleep}$ are leakage powers in active and sleep modes, respectively. Leakage energy equivalent time, $T_{\rm lkg\_eqv}$, can be defined as the active energy consumed by the switching operation being the same as the leakage energy saved by cutting off the block for that time

$$T_{\rm lkg\_eqv} \equiv \frac{E_{\rm switch}}{P_{\rm lkg} - P_{\rm sleep}}. \tag{1}$$

If a circuit block under sleep mode is woken up after $T_{\rm lkg\_eqv}$, cutting the block off decreases energy consumption. Otherwise, it consumes energy by toggling the cut-off switch. The leakage energy equivalent switching time in the Fig. 2 condition is 9.5ns. These simulation results indicate that turning off a given block can reduce leakage energy consumption if the block will not be reactivated within $T_{\rm lkg\_eqv}$. At least, if the probability of the reactivate within $T_{\rm lkg\_eqv}$ is less than 0.5, the system can statistically reduce energy consumption by leakage. Moreover, leakage current in the off-state MOSFET increases exponentially as $V_{\rm TH}$ decreases while active switching energy does not increase very much. As semiconductor technology scales down, the leakage power increases exponentially, resulting in shorter $T_{\rm lkg\_eqv}$.

Fig. 3 shows the trend of $T_{\rm lkg\_eqv}$ with the decrease of threshold voltage for 100-nm and 70-nm model parameters. Exponential decrease of $T_{\rm lkg\_eqv}$ can be seen with the decrease of threshold voltage and shrinking of gate length. The decrease of $T_{\rm lkg\_eqv}$ implies that the energy-saving probability by the leakage cut-off switch can be increased.

B. Locality of Block Activation in Time Domain

This paper is based on the fact that if a given block will not work for a longer time than the leakage energy equivalent time $(T_{\rm lkg\_eqv})$, turning the block off reduces energy consumption, while if the block is reactivated within $T_{\rm lkg\_eqv}$, turning the block off increases energy consumption. If the block is to be activated very soon, it is wise not to sleep. Unless the chip is for

Fig. 4. Block activation signals for two different applications of the 8-bit RISC microprocessor. (a) Application A: LCD driver. (b) Application B: Toy controller.

a well-defined job, such as an MPEG-4 decoder, we cannot predict whether a given block will be used soon or will not be used for long time. However, we found that there is a statistical behavior in the sleep duration. The proposed approach set a certain number of cycles before the sleep by using a self-timed circuit to determine whether the block should go into sleep mode or not.

An 8-bit RISC CPU is described using Verilog HDL to analyze distributions of interval times of block activation in real applications. Real application programs for an LCD driver and a toy controller are run. Fig. 4 shows the behaviors of important block activation signals for two different applications. Almost all the blocks can be activated by their block selection signals, or their activation signal can be easily generated in Verilog HDL. The adder in the ALU is hardly working in application A, while operating frequently in application B. The shifter in the ALU does not work at all in two applications. The results of this real application indicate that even if a chip is in active mode, some parts of the chip are not working or hardly working, and still consume energy by leakage.

The distribution of event intervals is derived to verify that the block activation has a time locality, that is, recently used blocks are more likely to be used again. Fig. 5 shows distributions of event interval for two applications. Here, *event interval* signifies the number of clocks between two adjacent block activations. The extracted statistical results show that the operation probability of a block is strongly dependent on previous events. In other words, it is more likely for a block to be operated if the block has been activated recently.

C. Criterion of Statistical Energy Saving

A criterion to enter the block into a sleep mode is derived to achieve the statistical energy saving effectively. Let us define $p(T_{\text{lkg\_eqv}} \,|\, T_{\text{wait}})$ as the conditional probability of activation within $T_{\text{lkg\_eqv}}$ on the condition that the activation signal has not been issued for T_{wait}, as shown in Fig. 6. This can be written as

$$p(T_{\text{lkg\_eqv}} \,|\, T_{\text{wait}}) \equiv \frac{p[T_{\text{wait}} \le t \le (T_{\text{wait}} + T_{\text{lkg\_eqv}})]}{1 - p(0 \le t \le T_{\text{wait}})} \quad (2)$$

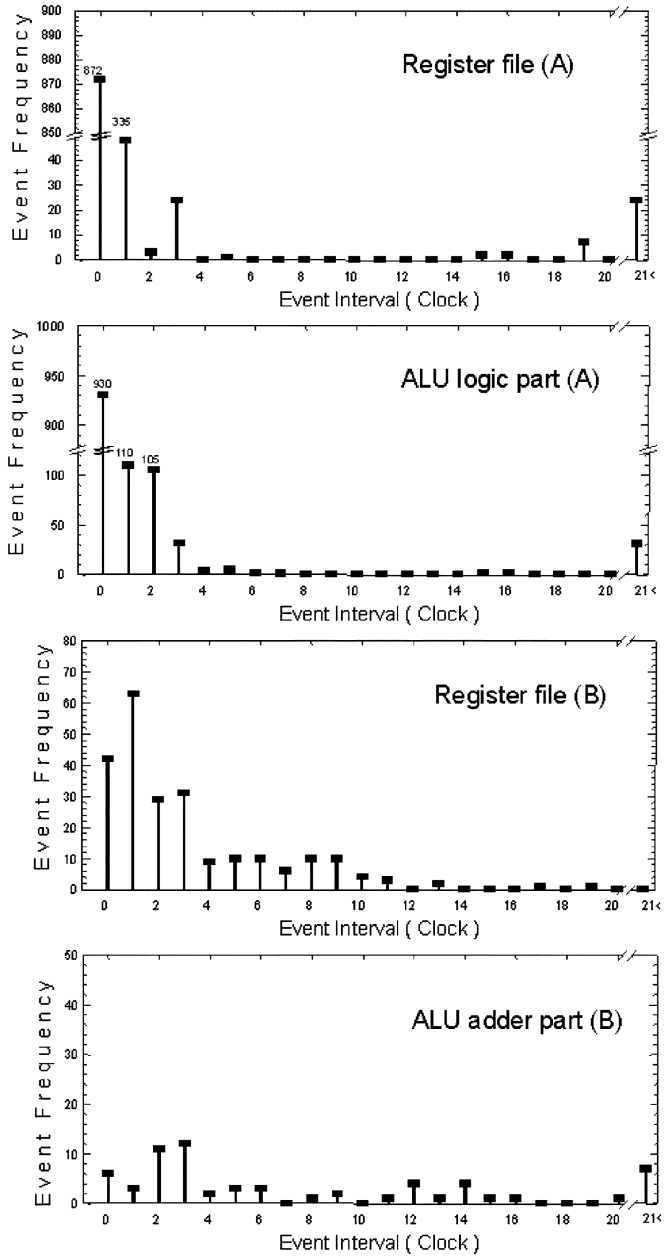


Fig. 5. Extracted event frequency as a function of event interval (the number of clocks between two adjacent block activations). A and B represent two applications, as shown in Fig. 4.

where $p(t)$ is the probability of block activation within time interval of t, and T_{wait} stands for the time interval between entering sleep mode and the latest block activation. A $p(T_{\text{lkg\_eqv}} \,|\, T_{\text{wait}})$ value of 0.5 means that the probability of block activation within $T_{\text{lkg\_eqv}}$ is 0.5 on the condition of entering sleep mode after T_{wait}.

Fig. 7 shows $p(T_{\text{lkg\_eqv}} \,|\, T_{\text{wait}})$ as a function of waiting time for the adder and the register file shown in Fig. 5 with two different $T_{\text{lkg\_eqv}}$. $p(10 \,|\, 5)$ is 2% for the adder unit and 8% for the register file. This means that the blocks will be reactivated within $T_{\text{lkg\_eqv}}$ time with the probability of 2% and 8%, when the adder and the register file enter the sleep mode after 5-clock waiting time. The activation probability decreases with decreasing $T_{\text{lkg\_eqv}}$ since the time window of $p(T_{\text{lkg\_eqv}} \,|\, T_{\text{wait}})$

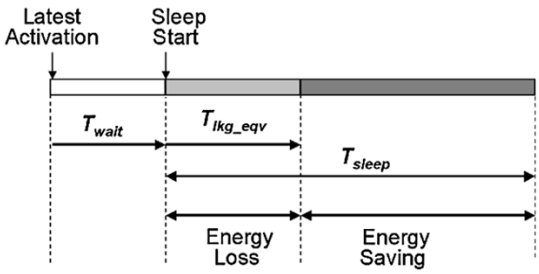


Fig. 6. Definition of notations to calculate a criterion of statistical energy saving.

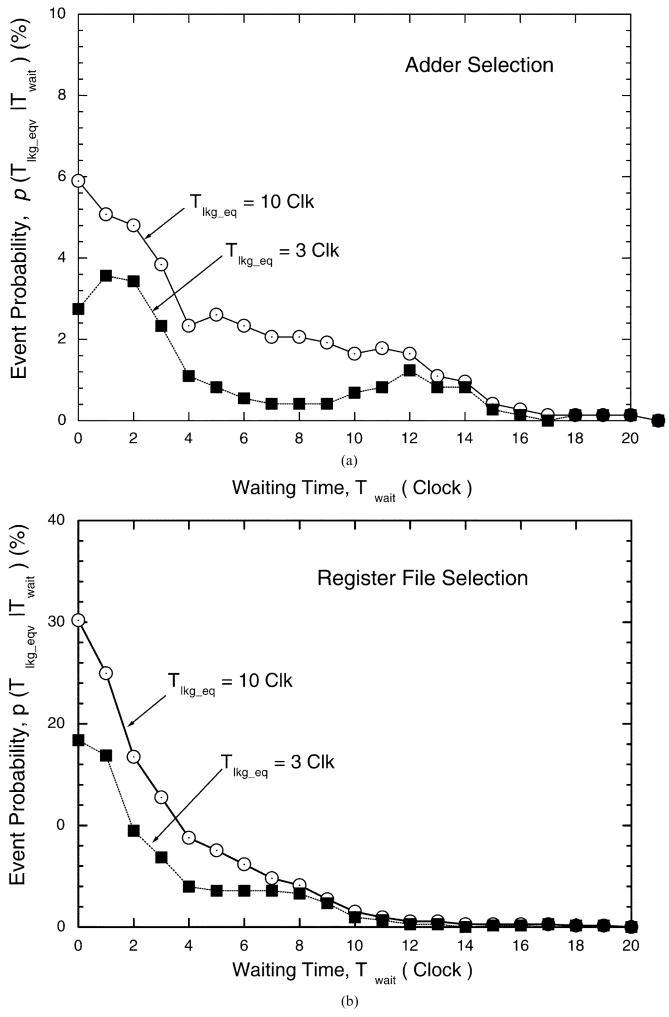


Fig. 7. Conditional probability of activation as a function of waiting time. Adder and register file of application B. (a) Adder. (b) Register file.

is shortened in (2). This implies that the proposed scheme is becoming more likely to reduce the leakage current as the devices go leaky.

D. Self-Timed Cut-Off Switch

Without issuing the sleep command from an internal control circuit or an external host command, a self-timed cut-off scheme is proposed to utilize locality characteristics of block activation in time domain. In this paper, a cut-off controller, shown in Fig. 8, is used as an example of implementing the

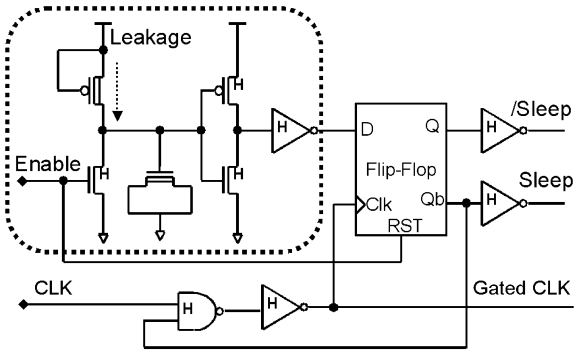


Fig. 8. Self-timed cut-off controller used in the simulations and experiments. Transistors marked H represent high threshold voltage transistors.

leakage current reduction by the self-timed cut-off switching scheme. Any sleep switching structures, such as MTCMOS, VTCMOS, and ZSCCMOS, can be used with the proposed switching controller.

The cut-off controller consists of a leakage integrator as a timer, a gated clock signal generator to suppress the conventional dynamic power by the clock, and one flip-flop to synchronize the sleep signal with the clock pulse and not to generate a glitch at the transition. Since entering sleep mode is not a timing-critical sequence, high $V_{\rm TH}$ is used to minimize the leakage caused by the switch itself, except the leakage-monitor PMOS and the capacitor.

The self-timed cut-off controller is very small in size. For example, it is 25 μm $\times$ 14 μm for 0.25-μm SOI technology except sleep signal drivers. Since the flip-flop and the NAND gate are needed anyway for the gated clock, the pure design overhead of the controller is the circuits in the dotted area in Fig. 8. The leakage current caused by this controller is less than 0.1% of the total adder leakage because it has 0.15 V higher threshold voltage and less than 1% of total gate area. Other than this controller, a cut-off switch itself and its signal driver are needed depending on switch scheme, such as MTCMOS, VTCMOS, ZSCCMOS, and other schemes.

III. Simulation and Measured Results

A. Simulated Leakage Current Behaviors

Fig. 9 shows part of the simulated leakage behaviors of a 64-bit CLA with the self-cut-off controller shown in Fig. 8. Waiting time of 27 ns and 5 ns are assumed. The signal pattern of block activation in the self-timed cut-off controller is taken by Verilog simulation using the firmware of application B. Simulation shows that the sleep signal generated by the self-timed cut-off controller is effective to reduce leakage current. Reactivation of the CLA just after entering sleep mode also can be seen, but the average energy consumption is statistically decreased by the proposed scheme.

Fig. 10 shows average leakage energy consumption of 64-bit CLA as a function of waiting time before entering sleep mode for 100-nm and 70-nm technology with the assumption of 500-MHz clock speed. The three different threshold voltage with L = 100-nm conditions are redrawn in Fig. 10(b) with more detailed energy scale to show the leakage behavior clearly.

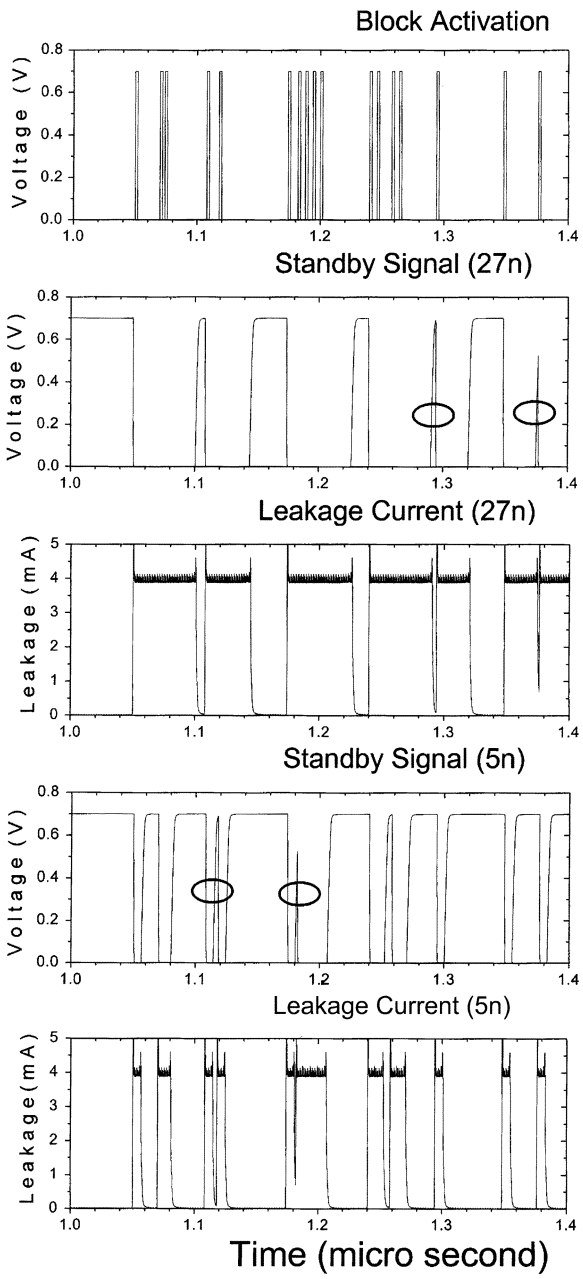


Fig. 9. Simulated leakage current behaviors of 64-bit CLA for application B with the self-timed cut-off controller shown in Fig. 8. Time conditions marked by a circle means energy-consuming events by the self-cut-off scheme. The others are energy-saving events.

The simulated results show about 75% active leakage reduction in 70-nm channel length with 0.13-V threshold voltage condition.

It is worthwhile to note that the leakage current slightly decreases with 25-ns waiting time in 100-nm channel length with 0.13-V threshold voltage condition, while it increases with the shorter waiting times than 25 ns, as shown in Fig. 10(b). This result means that the proposed scheme is very effective in active energy reduction for high leakage environments, but the efficiency of the proposed scheme is decreased with the leakage decrease, and even the energy consumption can be increased. Low leakage systems have long leakage equivalent sleep time, so that they can be less likely to save the leakage

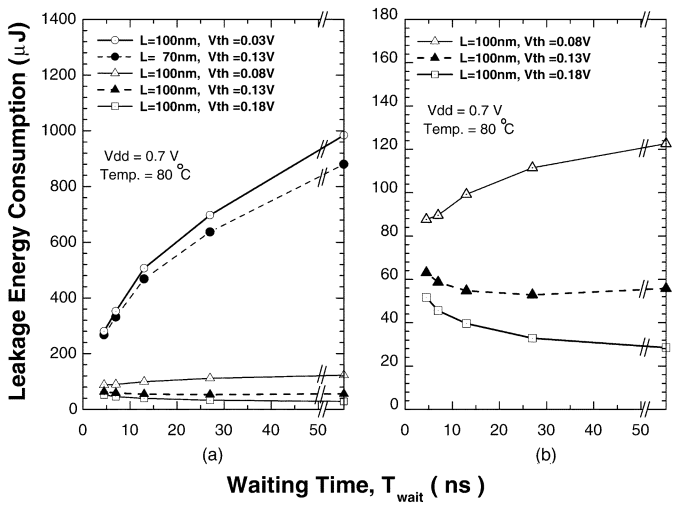


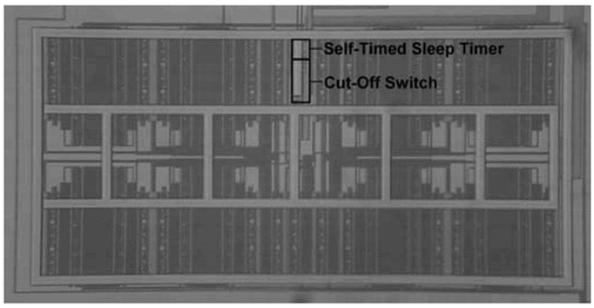
Fig. 10. (a) Simulated average leakage energy consumption of 64-bit CLA as a function of waiting time before entering sleep mode for application B with five different device conditions. (b) The three different threshold voltage conditions with $L = 100$ nm are redrawn with more detail energy scale.

current by cutting the block off, and more likely to consume energy with the switching operation. It is clearly seen from Fig. 10 that there is an optimum point for the waiting time before sleep. A criterion to determine the effectiveness is discussed in Section IV.

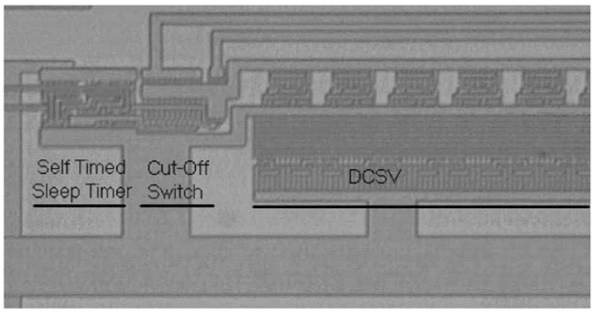
B. Measured Results

A test chip is fabricated by 0.25-μm dual-$V_{\rm TH}$ SOI technology. High and low threshold voltages of NMOS are 0.15 V and 0 V, and those of PMOS are -0.15 V and 0 V, respectively. A microphotograph of the fabricated chip is shown in Fig. 11. The test chip consists of a 64-bit carry-look-ahead adder of MTCMOS structure whose gate is controlled by the built-in self-timed cut-off controller. The layout size of the controller is less than 1% of the 64-bit MTCMOS full adder, but the total layout size is not increased since it is placed under the interconnections and power line, as shown in Fig. 11(a). The other test pattern with differential cascode voltage switch (DCVS) logic is also shown in Fig. 11(b). The block activation signal is generated by a pulse generator, and applied to the built-in self-timed cut-off controller. The gate bias of the PMOS leakage monitor in Fig. 8 is connected to an external pad to modify the waiting time for measurement purposes.

Fig. 12 shows measured average energy consumptions as a function of event interval with respect to various waiting times, $T_{\rm wait}$. The 64-bit CLA with 0-$V_{\rm TH}$ SOI transistors in this experiment shows 3-clock cycle of leakage equivalent sleep time with 50-MHz measuring clock speed. The measured results indicate that 3-clock waiting time with 20-clock activation interval saves leakage energy by 64% with the proposed method, while 4-clock activation interval shows an increase in energy consumption. The measured results demonstrate that the self-timed cut-off controller can optimize the total energy consumption by tuning the waiting time before sleep. If the event interval is distributed, the statistical energy saving can be determined by (2).



(a)



(b)

Fig. 11. Microphotographs of (a) fabricated test chip of 64-bit carry-look-ahead adder with self-timed cut-off switch, and (b) differential cascode voltage switch (DCVS) logic.

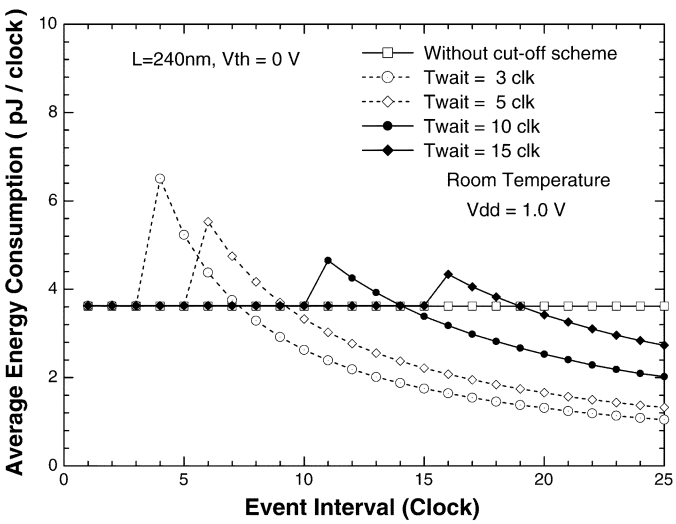


Fig. 12. Measured average energy consumption as a function of event interval with respect to various waiting times.

IV. Discussion

A. Wake-Up Within One Clock

If a block activation signal is asserted when the block is in a sleep mode, the circuit block should wake up quickly so as not to hinder the next operation. Recently, the zigzag super cut-off scheme (ZSCCMOS) has been proposed to shorten the waking-up time [10]. ZSCCMOS utilizes negative and/or higher voltage than $V_{\rm DD}$ to cut off leakage, while obtaining higher driving capability. In this paper, however, PMOS and NMOS cut-off switches have the higher $V_{\rm TH}$ instead of the super cut-off scheme originally proposed. Simulated wake-up time of the 64-bit carry-look-ahead adder is 0.60 ns for 100-nm device technology and the add operation can be executed just after the wake-up cycle.

B. Criterion of Effectiveness of the Self-Timed Cut-Off Switch

A criterion of the effectiveness of the proposed switch scheme is derived by the fact that the leakage energy per one clock $(E_{\rm lkg})$ multiplied by the average number of clock intervals $(T_{\rm av})$ should be larger than the activation energies of the block $(E_{\rm act})$ and switch $(E_{\rm swact})$ to achieve a benefit of energy saving by cut-off switch. This criterion can give the lower limit of the leaky environment. On the other hand, if $E_{\rm lkg}$ is larger than $E_{\rm act} + E_{\rm swact}$, the proposed self-timed cut-off scheme is not needed because the block can be turned off every nonoperating condition without the proposed self-timed controller. This can be the upper limit of the leaky environment. Let us define $\eta \equiv E_{\rm lkg}/E_{\rm act}$ that represents leakage energy ratio of the block with respect to active energy, and $\alpha \equiv E_{\rm swact}/E_{\rm act}$ that represents the overhead of active energy caused by controller itself. The derived criterion (η) is expressed as

$$\frac{1+\alpha}{T_{\rm av}} \leq \eta < 1+\alpha. \tag{3}$$

Under the above conditions, it is an advantage to apply the proposed self-timed cut-off scheme to save the leakage. Although a faster clock speed gives smaller leakage energy per one cycle with the same leakage conditions, the leakage increases more rapidly than any other performance parameters [2], so that the leakage energy saving technique becomes important.

V. Conclusion

A new leakage reduction scheme with self-timed cut-off controller is proposed as an effective leakage power reduction approach in active mode as well as in sleep mode. The proposed scheme utilizes a time locality of block activation of a given circuit blocks, and gives statistical leakage reduction by adjusting waiting time before entering sleep mode. The feasibility and effectiveness of the proposed scheme are verified by an 8-bit RISC microprocessor using Verilog HDL. The simulated data show a 75% active leakage reduction in 70-nm channel length with 0.13-V threshold voltage for the adder unit. A criterion of the effectiveness of the proposed method is also derived. Measured power saving of the 64-bit carry-look-ahead adder fabricated on 0.25-μm SOI also proves that the proposed method is efficient to reduce leakage current even if the chip is in active mode, as well as in sleep mode.

Acknowledgment

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Jin-Hyeok Choi (M'03) was born in Pohang, Korea, in 1967. He received the B.S., M.S., and Ph.D. degrees in electronics engineering from Seoul National University in 1989, 1991, and 1996, respectively.

In 1995, he joined the Memory R&D Center, Hynix Semiconductor Inc., Korea, where he worked on fabricating DRAM on SOI substrate and the circuit design of SRAM, DRAM, and Flash memory. He worked with the Institute of Industrial Science in the University of Tokyo, Japan, as a Research Assistant from February 2002 to March 2003. He has been working in the MCU Design Team of Samsung Electronics since April 2003. His research interests include high-speed and low-power circuit design with analog and digital mixed mode.

Yingxue Xu was born in Shanghai, China, in 1979. He received the B.S. degree in microelectronics from Fudan University, Shanghai, China, in 1998. He is currently working toward the M.S. degree in electronics engineering at the University of Tokyo, Tokyo, Japan.

His research interests are in the area of low-power CMOS digital circuits.

Takayasu Sakurai (S'77–M'78–SM'01–F'03) received the Ph.D. degree in electrical engineering from the University of Tokyo in 1981.

In 1981, he joined Toshiba Corporation, where he designed CMOS DRAM, SRAM, RISC processors, DSPs, and SoC solutions. He has worked extensively on interconnect delay and capacitance modeling known as the Sakurai model and alpha power-law MOS model. From 1988 to 1990, he was a visiting Researcher at the University of California, Berkeley, where he conducted research in the field of VLSI CAD. Since 1996, he has been a Professor at the University of Tokyo, working on low-power high-speed VLSI, memory design, interconnects, and wireless systems. He has published more than 250 technical papers, including more than 50 invited papers and several books, and holds 50 patents.

Dr. Sakurai has served as a Conference Chair for the Symposium on VLSI Circuits, and a technical program committee member for ISSCC, CICC, DAC, ICCAD, FPGA workshop, ISLPED, ASPDAC, TAU, and other international conferences. He was a keynote speaker for the 2003 ISSCC. He is an elected Administration Committee member for the IEEE Solid-State Circuits Society and an IEEE Circuits and Systems Society Distinguished Lecturer.