

90% Write Power Saving SRAM Using Sense-Amplifying Memory Cell

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Abstract

This paper describes a low power write scheme which reduces SRAM power by 90% by using seven-transistor sense-amplifying memory cells. By reducing the bit line swing to $V_{DD}/6$ and amplifying the voltage swing by a sense-amplifier structure in a memory cell, charging and discharging component of the power of the bit/data lines is reduced. A 64Kbit test chip has been fabricated and correct read/write operation has been verified. It is also shown that the scheme can also have capability of leakage power reduction with small modifications. Achievable leakage power reduction is estimated to be two orders of magnitude from SPICE simulation results.

Index Terms

SRAM, low power, write power, reduced swing, sense-amplifying cell, leakage current

I. Introduction

SRAM continues to be an important building block of System-on-a-Chips. Low power feature for on-chip SRAMs is getting more important especially for battery-operated portable applications. It is, however, also one of the most significant challenges of high-speed LSIs whose primary target is not low power but high performance. As systems become complex toward higher performance, on-chip SRAMs tend to have large number of bit width such as 16 to 256 or even greater. In this type of SRAMs, the active power of SRAM is dissipated mainly by charging and discharging of the highly capacitive bit/data lines, as is shown in Fig. 1(a), due to their full swing nature in write cycles. Therefore, power consumed in write cycles is much larger than that in read cycles. Figure 1(b) shows power estimation of 4Mb SRAMs having two different organizations. If bit width is 8, only 28% of the total power is consumed by driving bit/data lines. When bit width becomes 256, however, this value is lifted up to 90%.

Reducing voltage swing on the bit lines is an effective way to decrease the power dissipation in write cycles. In the Half Swing (HS) scheme [1], 75% power reduction was achieved by restricting the bit line swing to a half of V_{DD} in combination with charge recycling. It is, however, difficult to further reduce the power because of write-error problems in the HS scheme. HS scheme also has a problem in stable read operation because precharging bit lines to $V_{DD}/2$ in a read cycle increases possibility of erroneous flip of cell data. In fact, being different from DRAMs, half- V_{DD} precharging of bit lines has not been widely used in SRAMs. Therefore, $V_{DD}/2$ precharging in read cycles must be avoided. If bit-line voltage level in read cycles is lifted up from half- V_{DD} in the HS technique, another issue occurs. When the write and read cycles come alternately, there is additional power consumption for bit-line voltage recovery due to the mismatch of the voltage level of bit lines in read cycles and that in write cycles.

In this paper, a novel small-swing SRAM scheme using sense-amplifying cell is presented, with which further power saving in write cycles is possible. Since the write power is dominant in SRAMs with large bit width, the peak and average operation current can be reduced. The proposed scheme applies similar technique as used in the Driving Source Line (DSL) scheme reported in [2]. Two important difference between the two schemes will be explained in later sections. This paper also has two new contributions which were not included in [2]. First, several important trade-offs regarding the design of source-potential control circuit are discussed in detail with SPICE simulation results. Secondly, the effectiveness of small-swing write technique is verified with measurement results of a fabricated test chip, while only simulation results are given in [2].

This paper is organized by six sections. In section II, overall architecture of the SAC scheme is explained with detailed circuit diagrams and operation waveforms. The difference of the SAC scheme from the DSL scheme is also explained. In section III, quantitative analysis on design trade-offs is described with SPICE simulation results. It is also realized that these trade-offs are governed by two design parameters. In section IV, measurement results of the fabricated test chip are shown. In section V, possibility of cell leakage current reduction using the modified SAC scheme is explored, which was not included in the original paper [3]. In the final section, all discussions are summarized.

II. Sense-Amplifying Cell (SAC) Scheme

Figures 2 and 3 show the circuit diagram and the operation waveform of the proposed SAC scheme respectively. The salient feature of the scheme is an additional NMOS connected to the source of driver NMOS transistors in a memory cell, which enables small-swing of bit lines in a write operation. This additional NMOS is referred as “ V_{SS} switch” in the rest of this paper. A bit line is precharged to $V_{DD}-V_{TH}$ by an NMOS

load transistor and is pulled down to $V_{DD}-V_{TH}-\Delta V_{BL}$ in a write '0' operation, where V_{TH} and ΔV_{BL} are threshold voltage of the load NMOS and write swing respectively. The precharge level must not be V_{DD} because access transistors of the cell cannot turn on in the write operation in this scheme. There is no additional power consumption even if the write and read cycles come alternately, because there is no mismatch between the voltage level of bit lines in read cycles and that in write cycles. The SLC signal is synchronized with the word line signal WL, and the V_{SS} switch is turned off before WL goes up to high in a write cycle. Even if the voltage difference between a pair of bit lines is small, cell node can be inverted because the driver NMOS transistors do not draw current while the word line is activated thanks to the V_{SS} switch. After WL goes to low, SLC goes back to high and small-swing data is amplified to full-swing inside a cell. Note that all the cells connected to the activated word line should be written in a write cycle in this scheme. If the numbers of cells connected to a word line and to a SLC signal line are 64 and 256 respectively, for example, data stored in 192 cells become unstable while 64 cells are written.

The voltage level of $V_{DD}-V_{TH}-\Delta V_{BL}$ is prepared by a DC-DC converter with a help of voltage reference generator shown in Fig. 4(a). When an LC-type lossless DC-DC converter is used, power in bit/data lines of conventional SRAMs is reduced to $100 \cdot (\Delta V_{BL}/V_{DD})^2$ [%] due to the small bit-line swing of ΔV_{BL} . If a series regulator is used instead, achievable power saving remains around $100 \cdot (\Delta V_{BL}/V_{DD})$ [%] because of the regulator's power loss. LC-type DC-DC converter is, however, becoming popular in recent low-power digital ICs and is considered to be one of the most important building block for many ICs in the future. In the following discussions, the use of LC-type DC-DC converter is assumed. Therefore, when V_{DD} and ΔV_{BL} are set to 2.0V and 0.2V respectively, for example, the proposed scheme can save 99% of power consumed in bit/data lines in conventional SRAMs.

Small write swing also helps to reduce long write recovery time to charge bit/data lines up to precharge level. In conventional SRAMs, cycle time is usually determined by a write cycle. When ΔV_{BL} is reduced to 100mV, which is the same as typical voltage necessary between bit lines in a read cycle, write cycle time can be as short as read cycle time. Correct write operation with 100mV bit-line swing will be demonstrated in section IV. Since an SRAM cell has a high voltage gain, data swing recovery inside a cell does not cause cycle time penalty.

ΔV_{BL} must be independent of V_{TH} fluctuation in order to assure stable write operation. The voltage generator circuit shown in Fig. 4(a) can keep its output voltage V_{WR} equal to $V_{DD} - V_{TH} - \Delta V_{BL}$ even in the presence of V_{TH} fluctuation. Figure 4(b) shows ΔV_{BL} dependence of V_{TH} fluctuation realized by the circuit. When V_{TH} is fluctuated by $\pm 0.15V$, ΔV_{BL} fluctuation can be kept as low as $\pm 30mV$. V_{WR} is used as a reference voltage in the DC-DC converter and the converter supplies V_{WR} to each bit lines through the write circuit. Though the voltage generator consumes static current, only one generator is required in the whole SRAM chip and its power overhead is negligible.

Both the proposed SAC and the DSL [2] achieve small-swing write operation by setting source terminal of cell driver NMOS transistor floating in write cycles. Main advantages of the SAC scheme over the DSL scheme is avoidance of both half- V_{DD} precharging of bit lines and negative voltage. In the DSL scheme the source node of the cell driver NMOS transistor is driven to negative voltage during a read cycle in order to increase read current. This causes overstress on gate oxide of cell NMOS transistor and deteriorates device reliability, which becomes more serious issues in scaled devices. Avoidance of half- V_{DD} precharging of bit lines which is also used in the HS scheme is also preferable in terms of stable write operations because write error rate increases as bit-line voltage level decreases.

Another small-swing write technique, Switched Virtual-GND Level (SVGL) technique can be found in [4]. The difference between the SVGL scheme and ours are as follows. In the SVGL scheme, a source terminal of cell driver NMOS transistors is connected to a virtual-GND line, and its potential is increased from ground level during write cycles to achieve small-swing write operation. While a SLC signal line runs in parallel with a word line in the SAC scheme, a virtual-GND line in the SVGL scheme runs in parallel with a bit line. Since a bit line is usually longer than a local word line, overhead of driving the virtual-GND line in terms of delay, power and area is large when compared with those for driving the SLC signal line. In addition, when bit width is N , the number of activated virtual-GND line is equal to N , while the number of activated SLC signal line is 1. Thus, the SAC scheme can achieve lower power and higher speed than the SVGL scheme.

III. Cell Design Considerations

In SAC scheme, the primary concern in cell design are tradeoffs among read delay, noise margin and cell area. Before going into quantitative analysis of these three issues, it is explained that the tradeoffs are tightly related to two design parameters of the V_{SS} switch, β and N .

Figure 5 shows equivalent circuit of a sense-amplifying cell in a read cycle. Along the read current path, there are three NMOS transistors stacked. They are a cell access transistor, a cell driver transistor, and the V_{SS} switch, whose width are denoted as W_A , W_D and $W_{SW, 1CELL}$ respectively. By defining β as the ratio of $W_{SW, 1CELL}$ to W_D , the first key design parameter β is obtained. With such a definition, β becomes independent of technology-specific parameters and the following discussions can be applied to every technology node. In a conventional 6-transistor cell, W_D is set around $3 \cdot W_A$ and β is virtually infinite. According to the insertion of the V_{SS} switch having finite β value, read current and static noise margin will decrease. Therefore, it is clear that

larger β is better in terms of read delay and noise margin, but its maximum value is strictly limited by area constraints.

The second key parameter N is related to a layout issue of the V_{SS} switch. V_{SS} switch can not be placed cell by cell because area overhead goes beyond 20%. Therefore, it should be shared by a group of neighboring cells. In this case, there are three elements in each row which cause area penalty. They are the SLC signal line, the V_{SS} switch itself, and the common source line which connects each cell to the V_{SS} switch. If SLC signal lines are drawn with higher level metals, they cause almost no area overhead. Assuming that N cells share one common V_{SS} switch having transistor width of W_{SW} which is equal to $N \cdot \beta \cdot W_D$, more area-efficient layout is possible by increasing N . The most simple way is to set the value of N to its maximum same as the bit width. Such a configuration is, however, impossible in practice due to the following reason. Figure 6 shows read current path in the shared V_{SS} switch structure. When read current I_R flows through each cell in read cycles, the maximum current through the common source line is as large as $N \cdot I_R$. The minimum width necessary for avoiding electromigration is approximately N times larger than that of a bit line. Such a wide metal line, however, can not be drawn within the row pitch. For a typical SRAM cell layout whose bit-line width is 1/4 of a cell width and whose cell height is twice larger than cell width, the minimum width of a common source line becomes larger than the cell height if N is larger than 8. Thus, in practice maximum number for N is around 8. In the rest of this paper, only these three N values, 2, 4, and 8 are used for trade-off analysis. It should be also noted that in DSL [2], width of a source line and a word line are comparable, but such a thin line can not be used with the same reason described above.

Figure 7 and 8 shows simulated read delay and noise margin with respect to β . Here, a 4Mbit SRAM is assumed. The read delay is defined by the delay from address buffer input to output buffer output. Noise

margin is defined as length of a diagonal line of the maximum square in the area bounded by the transfer curve of the memory cell and its 45-degree mirror as shown in Fig. 8. From the figures 7 and 8, it is understood that decreasing β degrades both read delay and noise margin, and that they are almost insensitive to the number N .

Figure 9 shows area overhead as a function of β value. All cell areas are normalized by that of a conventional 6-transistor cell. Cell area is calculated by drawing cell array layout for each N . In the graph, cell area occupancy is assumed to be 60% of the total area of the SRAM macro. When N is 2, area overhead is always larger than 10%, while it can be kept below 10% when N is 4 and β is 4 or less. When N is 8, however, a sufficiently wide metal line could not be drawn for the common source line within the row pitch. Considering these simulation results, $\beta=3$ and $N=4$ are chosen in the test chip design, which corresponds to 5% read delay increase, 25% noise margin decrease and 11% area increase.

IV. Measurement Results

A test chip of 64K bit SRAM was fabricated with 0.35 μ m triple-metal CMOS process. Figure 10 shows a microphotograph and layout of the cell array. In the test chip, first metal layer is used for cell V_{DD} lines, word lines and local connections inside a cell. Second metal layer is used for bit lines and mesh-structured V_{SS} lines. Third metal layer is used for common source lines and SLC signal lines. One V_{SS} switch is inserted at the center of each 4 cells as is shown in Fig. 10. The SRAM test chip operated at 100MHz with 1.5V supply. The features of the chip and the technology are summarized in Table I.

Measured and simulated ΔV_{BL} dependence of bit line power is plotted in Fig. 11. Power dissipation of 125mW in full swing write is reduced to 4.2mW when ΔV_{BL} is lowered to $V_{DD}/6$ of 250mV. Figure 12 shows relationship between bit width and total power consumption in a write cycle. The more the bit width is, the

more the total write power is saved because the power consumed by charging and discharging of bit lines becomes more dominant compared with the power of the other circuits when the bit width gets larger. When the bit width is 256, total write power saving of the proposed SAC scheme is 90% for the conventional full swing scheme, and 67% for the HS scheme.

V. Cell leakage reduction with the SAC scheme

As transistors are scaled, both V_{DD} and V_{TH} are scaled. In sub 1V region, V_{TH} will be 0.2V or less. In that case, due to exponential dependence of leakage current on V_{TH} , more than 99.9% of un-accessed cells become the dominant power consumer even in active mode as pointed out in [5]. For solving this problem, two different schemes, Dynamic Leakage Cutoff (DLC) scheme [6] and Row-by-Row Dynamic V_{DD} (RRDV) scheme [7], are proposed. In the DLC scheme, subthreshold leakage current of cells is reduced by using substrate bias effects, while in the RRDV scheme, it is reduced by using Drain Induced Barrier Lowering (DIBL) effects in conjunction with negative word line. What is in common with these schemes is that leakage power is controlled row by row with an additional power control signal synchronized with a word line. Since the SAC scheme has SLC signal for each row, it can also have capability of leakage power reduction with only slight modifications. The fundamental idea behind the modified SAC scheme is reducing leakage current by DIBL effects, being similar to the RRDV scheme. The circuit implementation of the modified SAC scheme and trade-offs between these two schemes are explained below.

Figure 13 shows an example of circuit implementation of a V_{SS} switch controller and its truth table in the modified SAC scheme. In write cycles, the waveform of the common source line in the modified SAC scheme is the same as that in the original SAC scheme described in section II, but in read cycles they become different. The operation waveform in a read cycle is shown in Fig. 14. The cycle time can be divided into two parts

depending on whether word line is high or low. While word line is low, voltage on the common source line goes up to V_{DDL} and cell stores data at reduced voltage swing of $V_{DD} - V_{DDL}$. When reduced voltage is applied to a cell, leakage current from cell V_{DD} is reduced by DIBL effects, which is a specific phenomenon in deep submicron transistors. When voltage applied to a cell is decreased, cell stability becomes an issue, which is beyond the scope of this paper. It is reported in [8], however, that cell data can be stored at around 0.2V with careful design. In 70nm technology node, for example, it is shown from SPICE simulation with predicted transistor models [9] that leakage current from cell V_{DD} is estimated to be decreased to 20% or less when V_{DDL} is changed from 0.0V to 0.8V for supply voltage of 1.0V.

Another considerable leakage source in an SRAM cell is a precharged bit line. Leakage current flowing into a cell from bit lines is typically between 10% and 20% of leakage current from a cell V_{DD} line. Once leakage current from cell V_{DD} is reduced, bit-line leakage becomes dominant. Bit-line leakage should also be suppressed for assuring stable read operation [10]. The modified SAC scheme suppresses bit-line leakage without negative voltage, which is used in the RRDV scheme. Figure 15 shows an equivalent circuit of an unaccessed cell. When a common source line goes up to V_{DDL} , voltage on node N2 also goes up to V_{DDL} , and negative V_{GS} is automatically applied to the access transistor M_{ACC} . This situation is equivalent to increasing V_{TH} of M_{ACC} by V_{DDL} . Therefore, bit line leakage becomes negligibly small. The voltage level of V_{DDL} can be same as V_{WR} supplied from the DC-DC converter used for reduced swing write technique described in section II. In that case there is no need to prepare additional voltage generator. Higher V_{DDL} can further lower both write power and cell leakage power. Achievable total leakage reduction with this modified scheme is almost same as that of RRDV, and is estimated to be two orders of magnitude.

The difference between the RRDV scheme and the modified SAC scheme is as follows. In the RRDV scheme, data swing of a cell is controlled from V_{DD} side, but in the modified SAC scheme, it is controlled from V_{SS} side. When cell swing is controlled from V_{DD} side, the small-swing write technique described in Section II can not be applied. RRDV also requires negative voltage on inactive word lines for suppressing bit-line leakage current. If negative voltage is used in the circuit, however, additional voltage generator such as a charge pump circuit should be integrated. In addition, in order to avoid overstress on transistor gate oxide, some peripheral circuits such as word line drivers and write drivers should be modified as described in [7]. Contrary to the RRDV scheme, both write and leakage power can be saved without these design change.

Leakage current reduction of an SRAM cell with similar voltage-controlling method can also be found in the recently published paper [11], but there are three essential differences from the proposed scheme. First of all, leakage reduction mechanism in [11] works only when the whole chip enters standby mode. Therefore, the method is no good for reducing leakage power in an active mode. Secondly, voltage level of common source line is not controlled row by row but bank by bank, where one bank is composed of many rows and columns. Such a configuration can not be implemented in the SAC scheme. Let us assume that one row inside one bank is accessed in a write cycle. The common source line of the bank becomes floating. This will corrupt data of cells on other rows inside the same bank. Finally, bit-line voltage is reduced in [11] depending on whether in active mode or standby mode. If bit-line voltage is dynamically controlled during active mode, however, it will consume large active power and the merits of small-swing write operation will diminish.

VI. Conclusion

Sense amplifying cell (SAC) scheme is presented for wide-bit SRAMs. A test chip was designed and fabricated in 0.35 μ m CMOS technology, and a correct read/write operation was verified. 90% of power in

write cycles is saved by using the small-swing bit-line scheme. As a guide for practical design, it is shown that trade-offs among area, delay and noise margin are governed by two design parameters, β and N , associated with the V_{SS} switch. Decreasing β save layout area but degrade both noise margin and read delay. Increasing N for a given β can also save layout area, but when taking electromigration into account, practical design should choose N around or less than 8 so that enough wide metal can be drawn for a common source line within a cell pitch. Assuming 4M bit SRAM, the delay overhead and area overhead of the scheme are estimated to be 5% and 11% respectively when β is 3 and N is 8. Difference between the proposed scheme and other small-swing write techniques are also discussed in detail. Two main advantages are avoidance of half- V_{DD} precharging of bit-lines and negative voltage on cell source lines. With these advantages, the SAC scheme can save more write power without degrading cell stability and device reliability. Possibility of reducing leakage power of unaccessed cells during active mode by slightly modifying the SAC scheme is also explored. In the modified SAC scheme, leakage current from cell VDD lines is reduced by DIBL effects, while leakage current from bit-lines is automatically suppressed when voltage on the source node of cell driver transistors goes up. Like the RRDV scheme in [7], leakage power can be saved by two orders of magnitude.

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Figure Captions

- Fig. 1 Write power consumption in conventional SRAMs. (a) Capacitive load on bit/data lines. (b) Write power comparison between two different SRAM configurations.
- Fig. 2 Overall architecture of SAC scheme.
- Fig. 3 Write cycle waveform.
- Fig. 4 Write voltage generator design. (a) Circuit diagram. (b) Output voltage fluctuation against V_{TH} variations.
- Fig. 5 Read current path of a 7-transistor cell in a read cycle.
- Fig. 6 V_{SS} switch layout considerations. (a) Read current path in shared- V_{SS} switch structure. (b) Division of a source line.
- Fig. 7 Simulated β dependence of read delay.
- Fig. 8 Simulated β dependence of cell static noise margin.
- Fig. 9 Relationship between β and area overhead.
- Fig. 10 Chip microphotograph and cell layout.
- Fig. 11 Relation between bit line swing ΔV_{BL} and power consumption in bit lines and cells.
- Fig. 12 Relation between bit width and total write power consumption.
- Fig. 13 Circuit diagram of a V_{SS} switch controller and its truth table.
- Fig. 14 Read cycle waveform in the modified SAC scheme.

Fig. 15 Equivalent circuit of an un-accessed cell.

Table I Test chip summary.

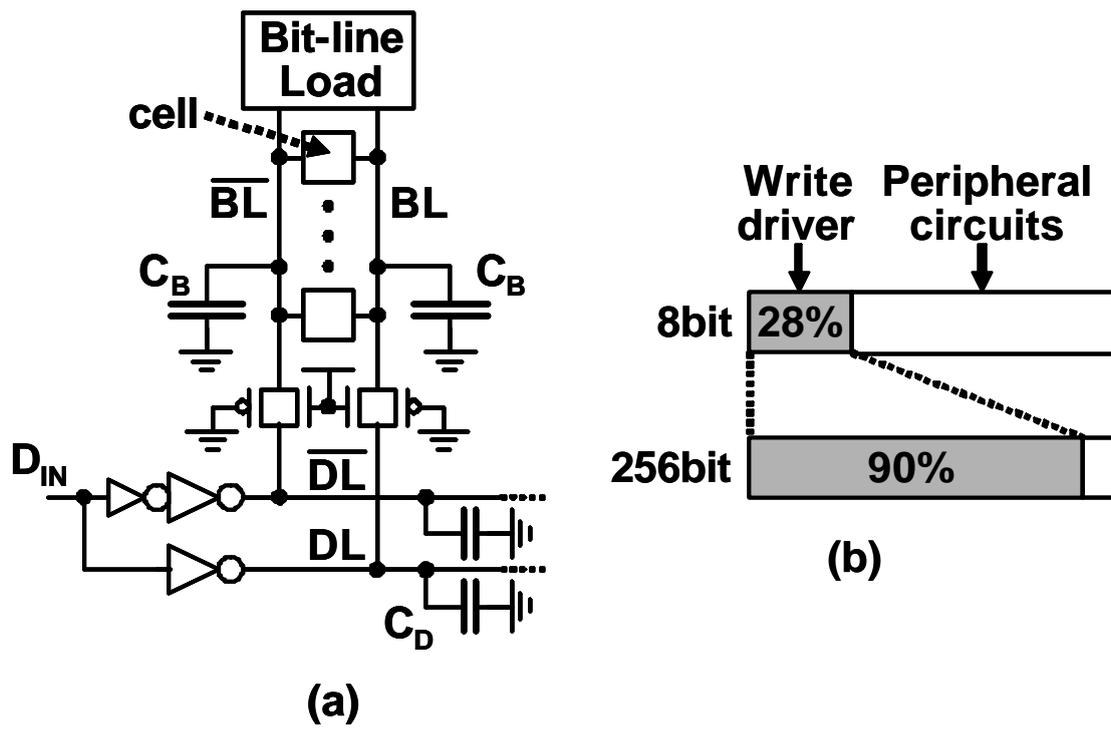


Fig. 1

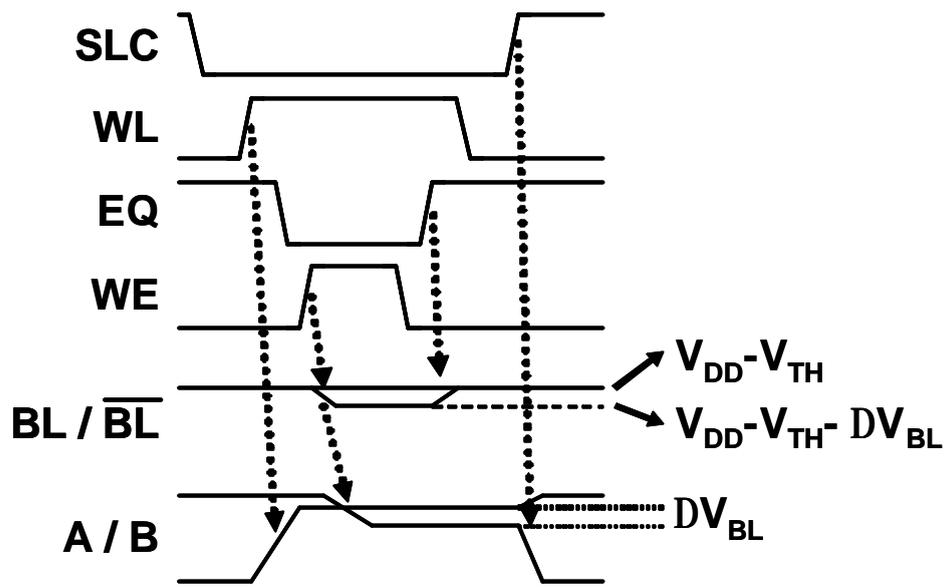
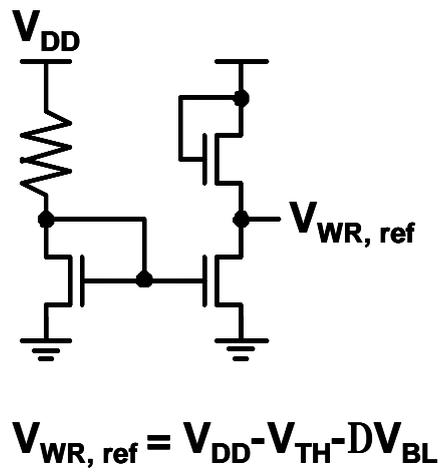
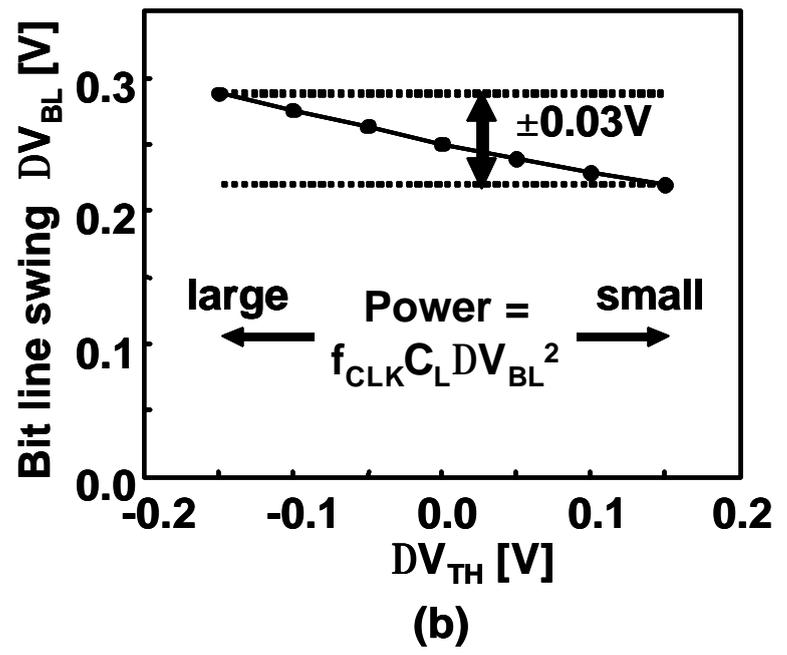


Fig. 3

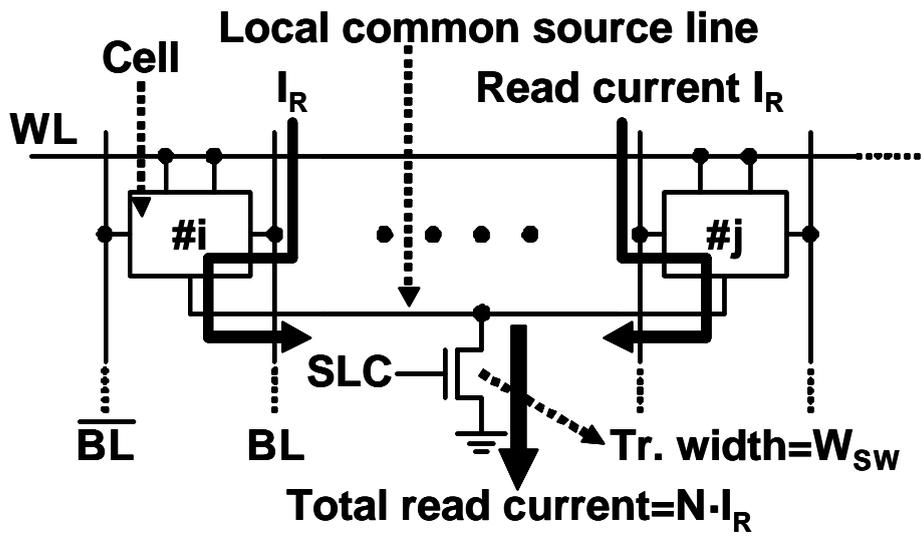


(a)

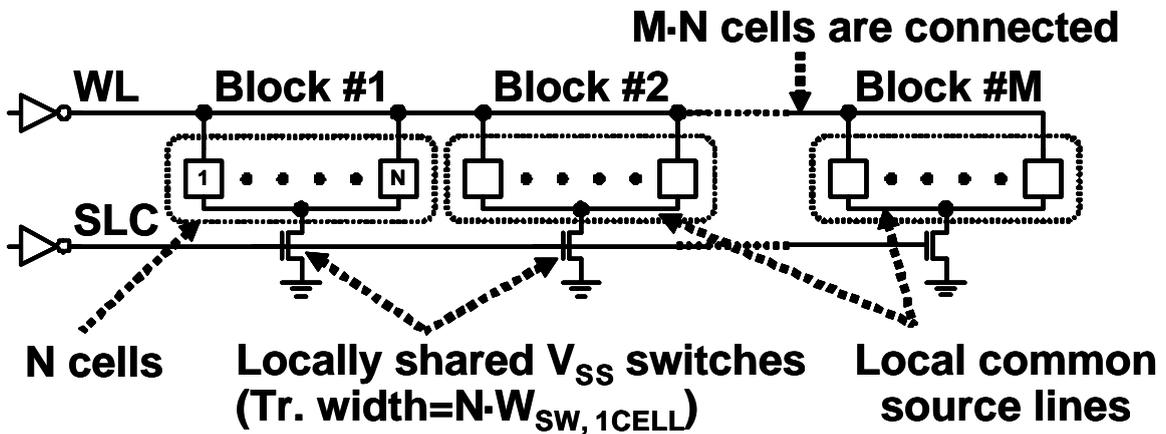


(b)

Fig. 4



(a)



(b)

Fig. 6

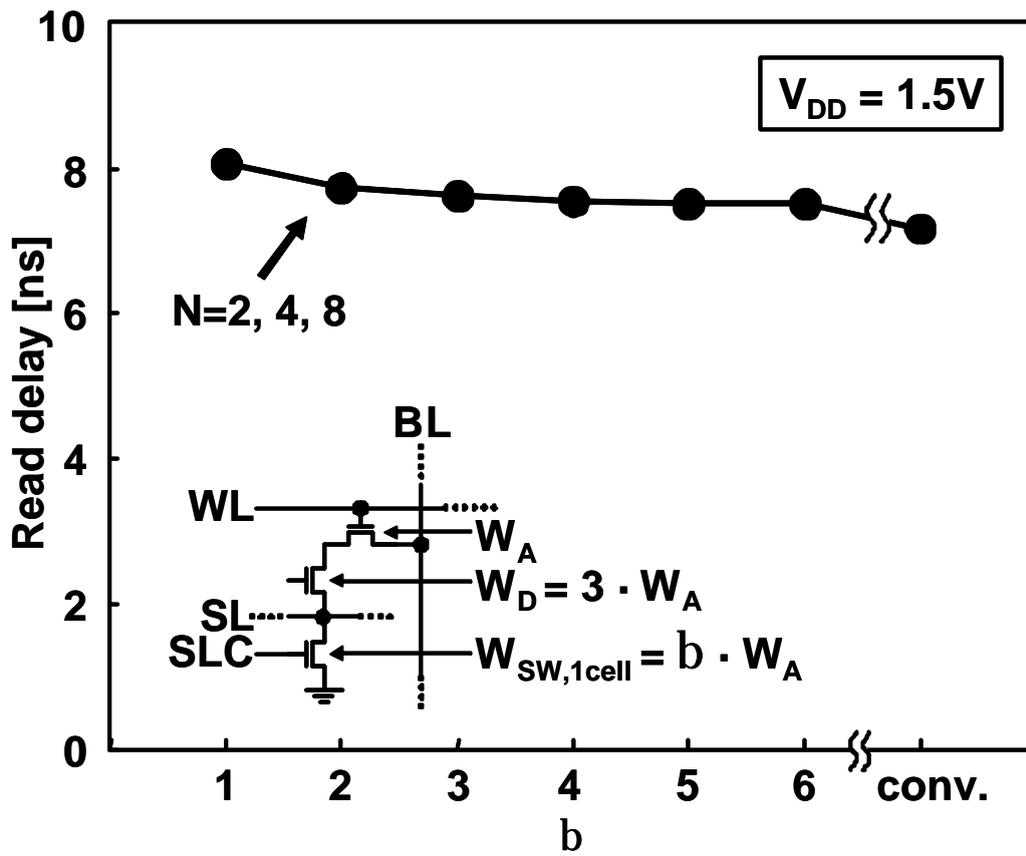


Fig. 7

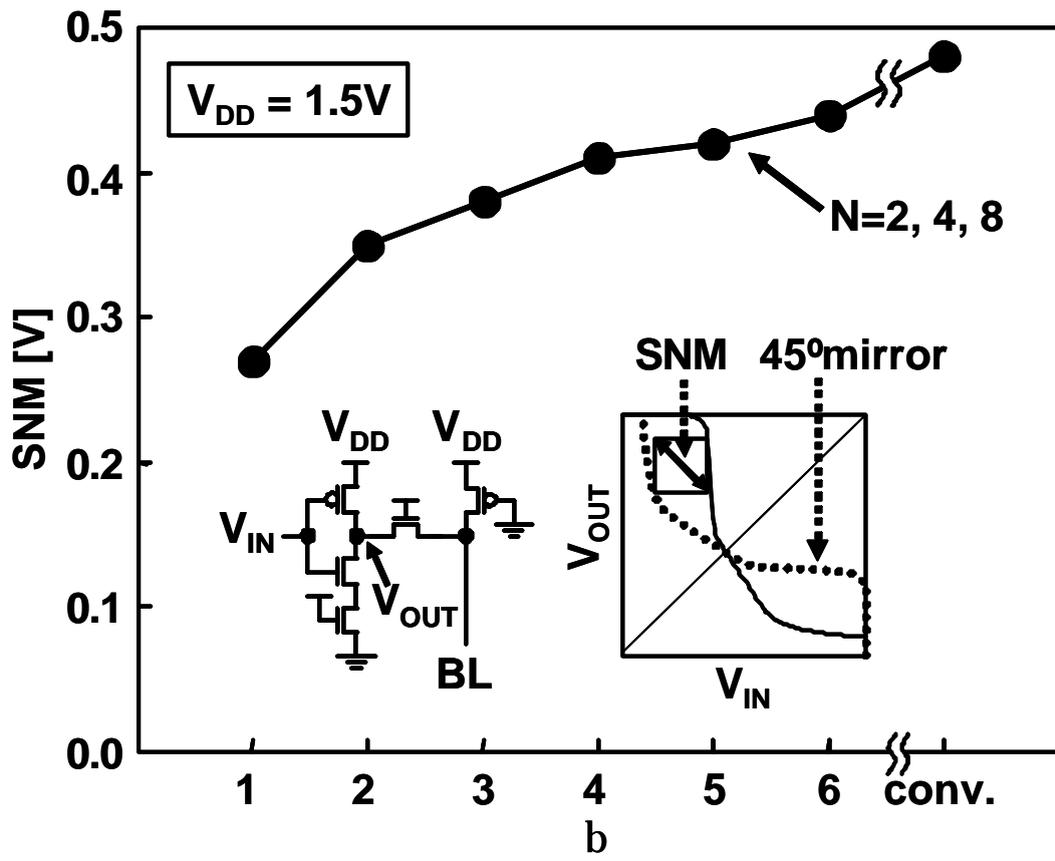


Fig. 8

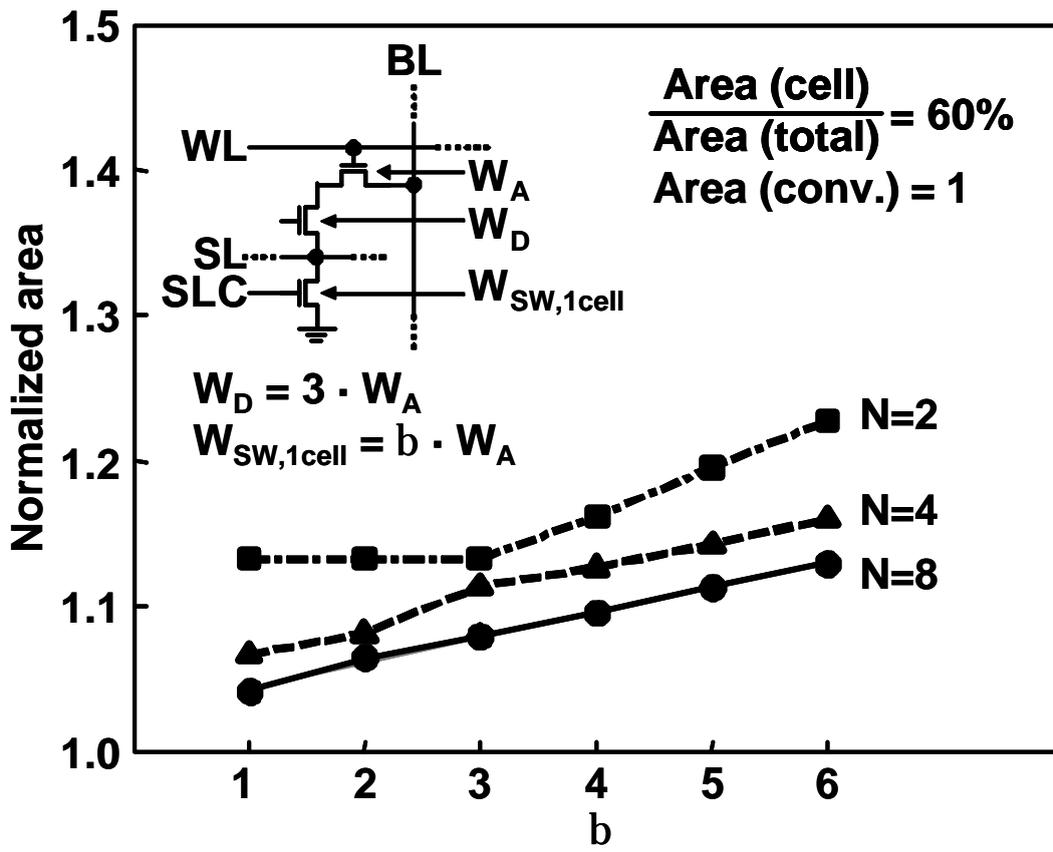


Fig. 9

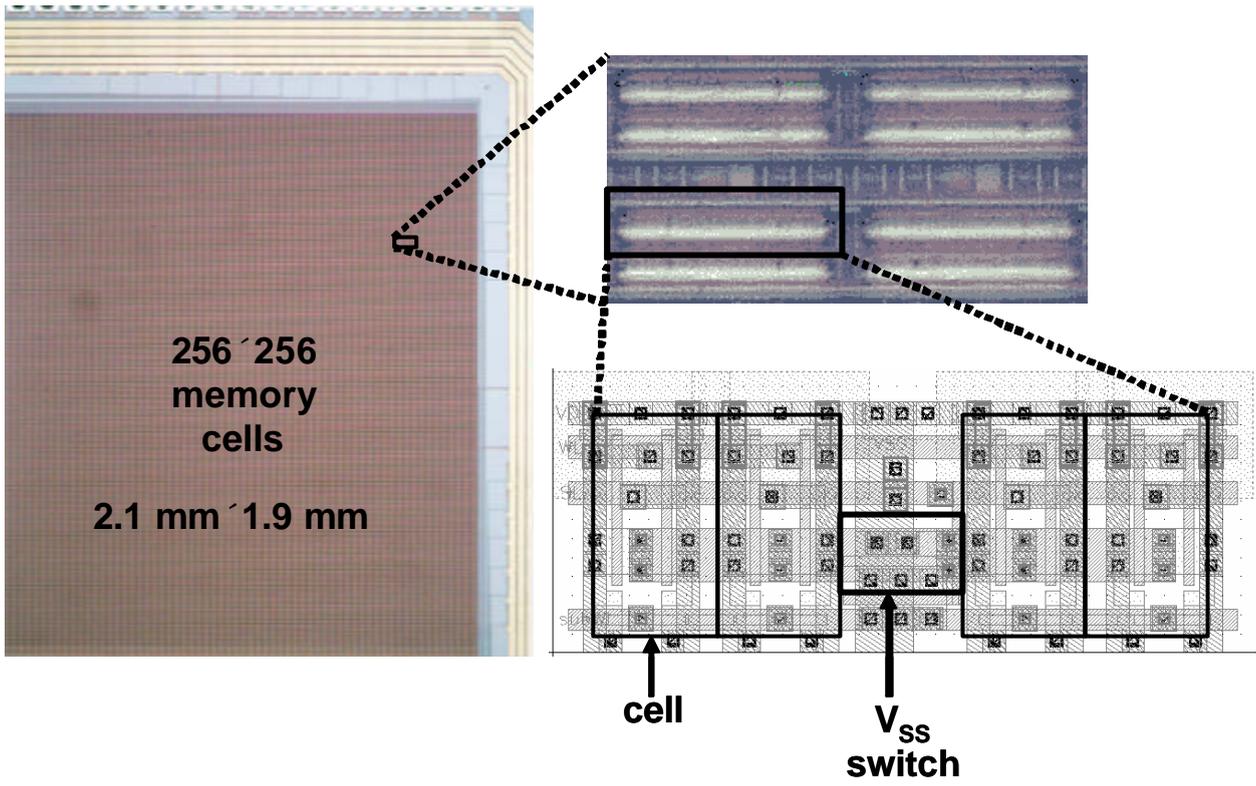


Fig. 10

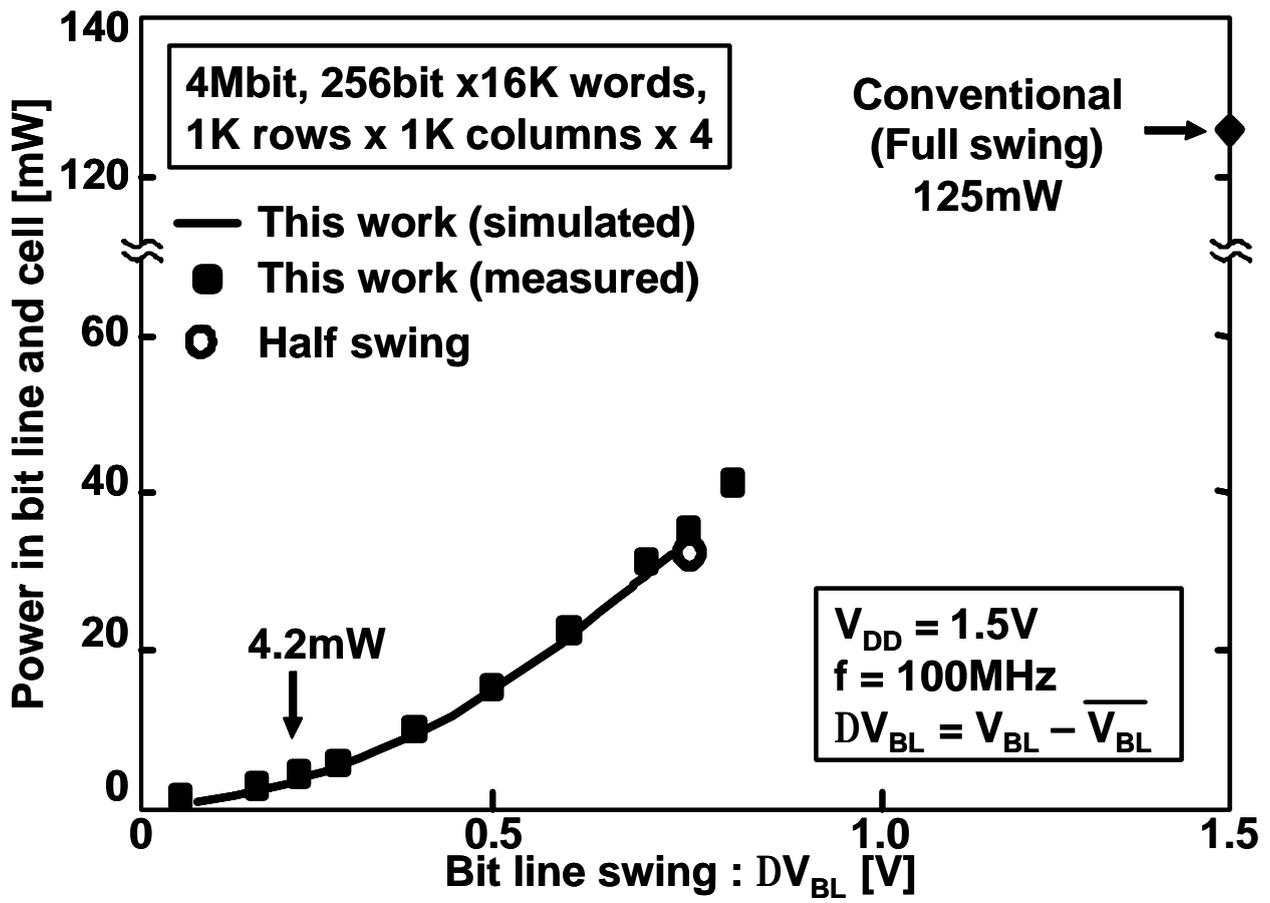


Fig. 11

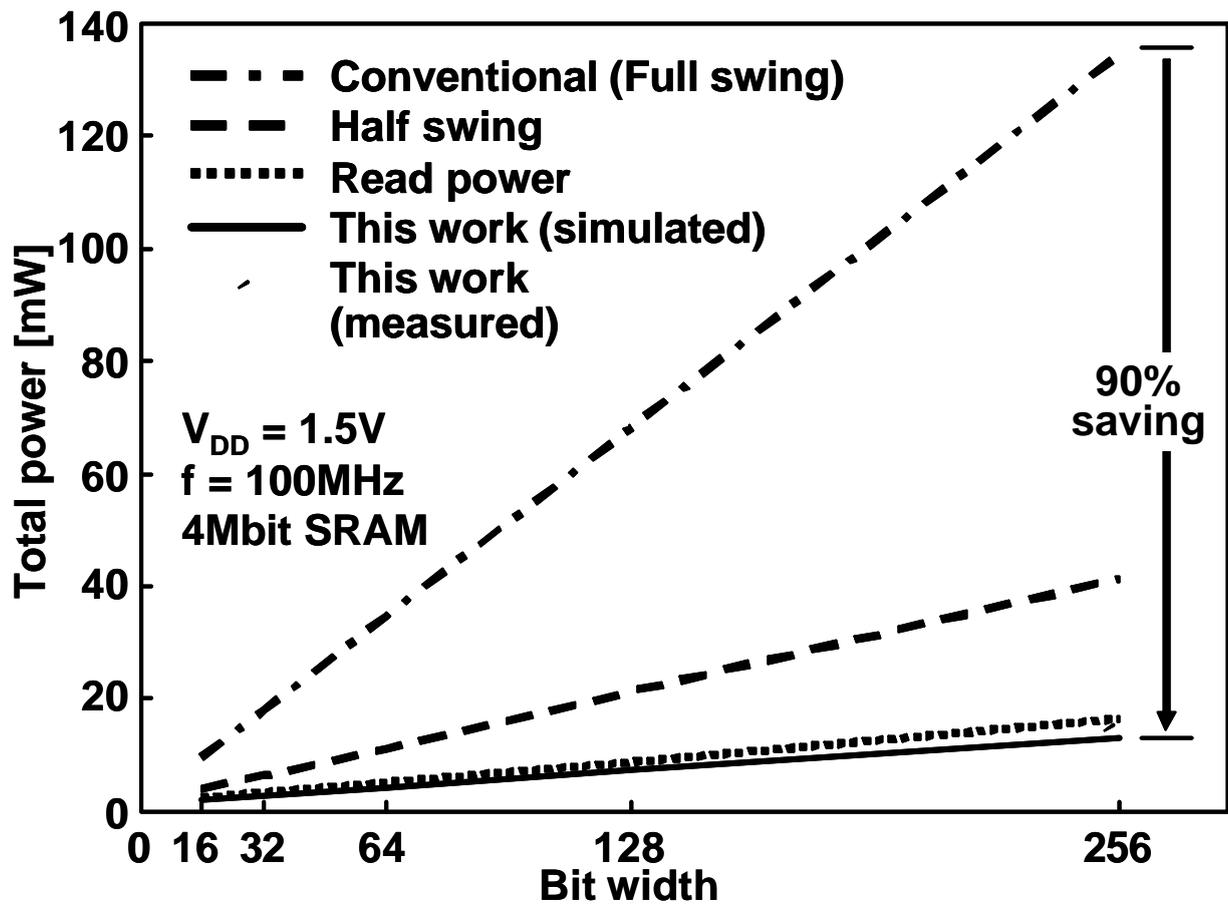
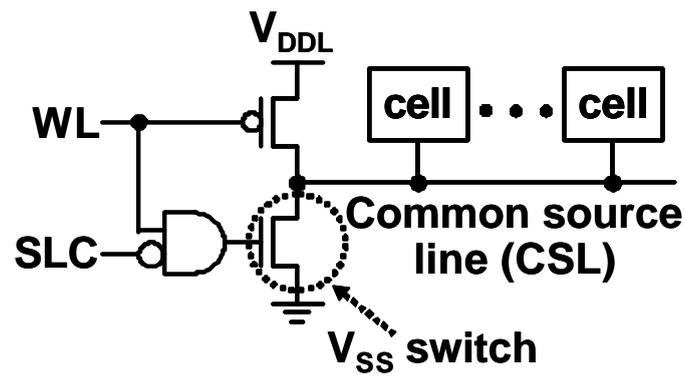


Fig. 12



WL	SLC	CSL	Mode
0	0	V_{DDL}	Retention
0	1	V_{DDL}	Retention
1	0	0	Read
1	1	HiZ	Write

Fig. 13

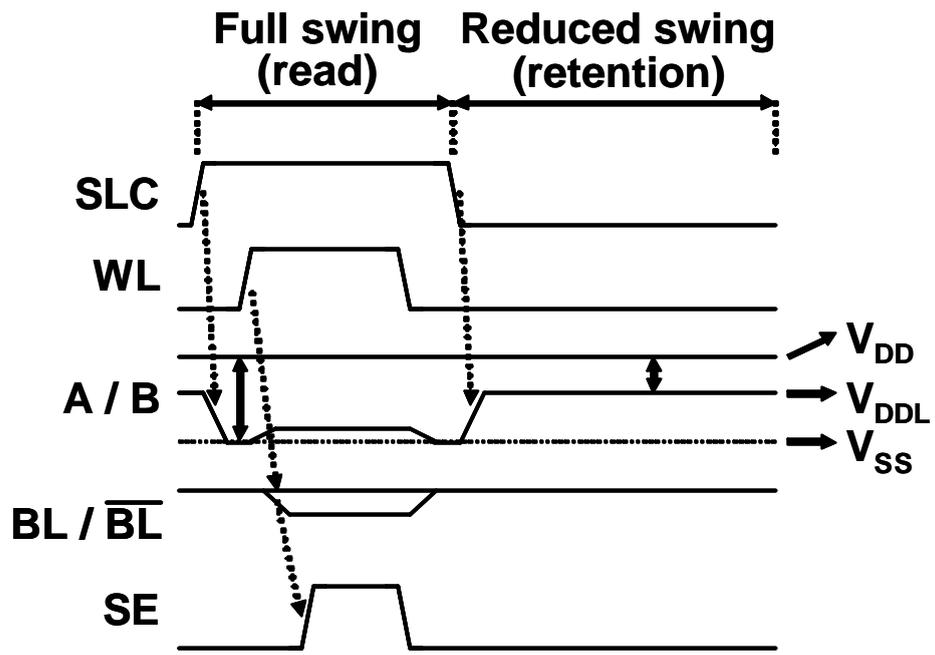


Fig. 14

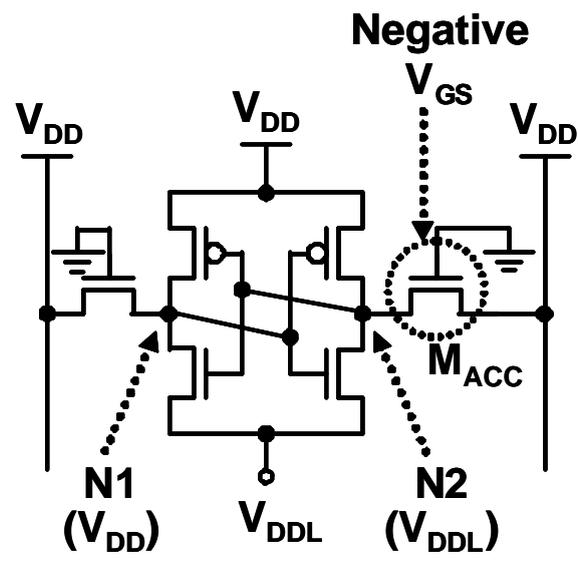


Fig. 15

TABLE I

Technology	0.35 μ m CMOS, triple-metal
SRAM	64Kb (256 rows & columns)
Supply voltage	1.5V
Operation frequency	100MHz
Write power(@256bit)	13.6mW ($\Delta V_{BL}=250$ mV)
	135mW ($\Delta V_{BL}=1.5$ V)