

Perspectives in Power-Aware and Large-Area Integrated Circuits for Ubiquitous Electronics

Takayasu Sakurai

Center for Collaborative Research, and Institute of Industrial Science, University of Tokyo
4-6-1 Komaba, Meguro-ku, Tokyo, Japan, 153-8505
tsakurai@iis.u-tokyo.ac.jp, <http://lowpower.iis.u-tokyo.ac.jp/>

Abstract — In the forthcoming ubiquitous electronics age, power-aware VLSI's and large-area electronics are of importance. If electronics does not provide low-power solutions, the power consumption of hardware will eat up the energy of the community. Large-area electronics is critically in need, since ubiquitous electronics needs to interact with people with sensors and actuators. The paper describes the recent topics in low-power VLSI systems and the possibility of large-area electronics by organic transistors.

Keywords — VLSI, Low-power, Large-area, Organic

I. SUMMARY

In the coming ubiquitous IT society, low-power design is one of the key features at which the VLSI designer should aim. Otherwise, power increase will remain as one of the main obstacles to Moore's law growth. Unless VLSI power is lowered by orders of magnitude, we cannot enjoy the progress that scaling offers. This talk will cover what we now have, and what we should provide in our low-power armory to allow us to cope with ever-increasing leakage loss, as well as dynamic power. The techniques to be presented range over the system, software, circuit, and device level including interconnect and I/O issues. The novel trend is to examine cooperative approaches between levels such as software-circuit cooperation and circuit-technology cooperation. The biggest challenge that System-on-Chip designers must resolve in the future is the fact that transistors for digital and memory circuits will be more and more leaky as technology generations advance. Approaches to solving this serious problem will be described. Beyond the quest for low-power solutions lies a promising world of ubiquitous VLSI devices and products ranging from "wireless sensors and tags for everything" to "everything-you-can-do mobile terminals". (see Figs.1-22, and refer to [1-5])

Another technology of interest is large-area electronics, since ubiquitous electronics needs to interact with people with sensors and actuators. Organic electronics may be suitable for the objective. A large-area pressure sensor matrix has been fabricated on a plastic sheet for the first time, integrating high-quality organic field-effect transistors and rubbery pressure sensors. This pressure sensor demonstrates the feasibility of applying the organic transistor technology to flexible area-sensors, which opens up new applications of organic FET's

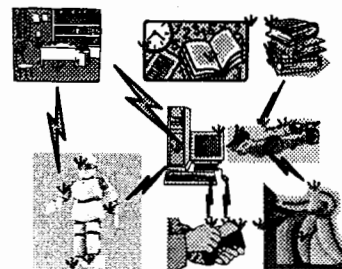
including artificial skins. (see Figs. 23-25 and refer to [6-7])

ACKNOWLEDGEMENT

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RFID node
Sensor node
Storage node
Computing node
Networking node
Actuator node
Display node

Intel CTO: Dr. Pat Gelsinger

センサ・ネットワーク技術に取られることで、すぐに収益を得られるわけではない。ただその将来性は大きい。当社の組み込みマイコン製品が持つ年間数十億ドルという収益規模を、センサ・ネットワーク関連製品ははるかにしのぐことになるだろう。だからこそ取り組んでいる。

日経エレクトロニクス2002.5.20 p.192

US: Wireless sensor network
Europe: Ambient intelligence

Fig.1 New infrastructure: ubiquitous electronics

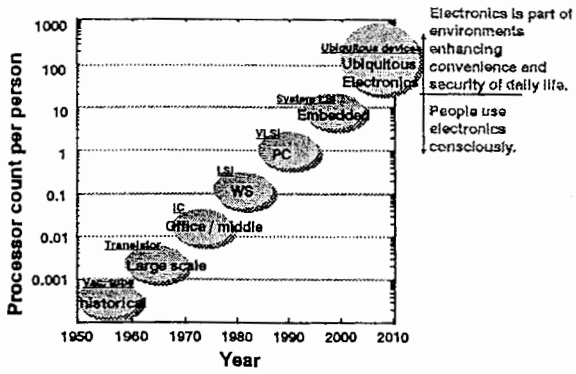


Fig.2 Ubiquitous electronics is natural extension

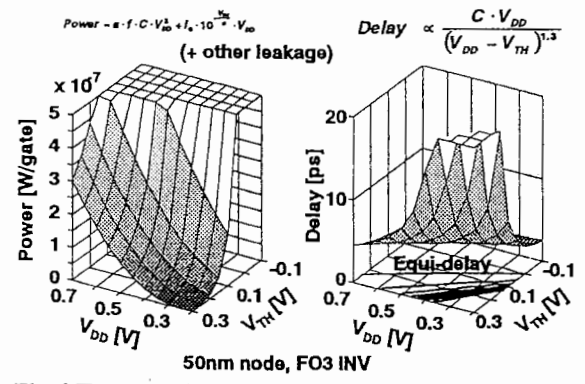


Fig.6 Trade-off between power and delay

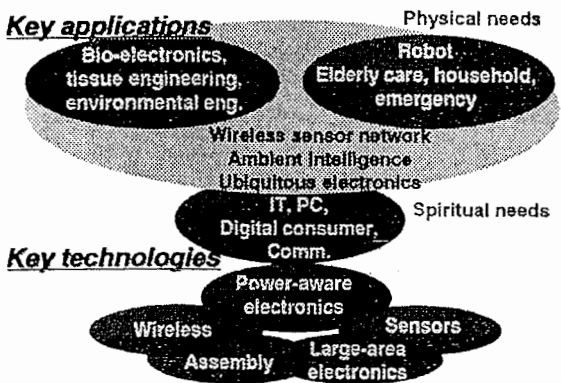


Fig.3 Ubiquitous electronics and key technologies

	Active	Stand-by
Multiple V_{TH}	Dual- V_{TH}	MTCMOS
Variable V_{TH}	V_{TH} hopping	VTCMOS
Multiple V_{DD}	Dual- V_{DD}	Boosted gate MOS
Variable V_{DD}	V_{DD} hopping	

Software-hardware cooperation (points to Variable V_{DD})
Technology-circuit cooperation (points to Boosted gate MOS)

- * MTCMOS: Multi-Threshold CMOS
- * VTCMOS: Variable Threshold CMOS
- Multiple : spatial assignment
- Variable : temporal assignment

Fig.7 Controlling VDD and VTH for low power

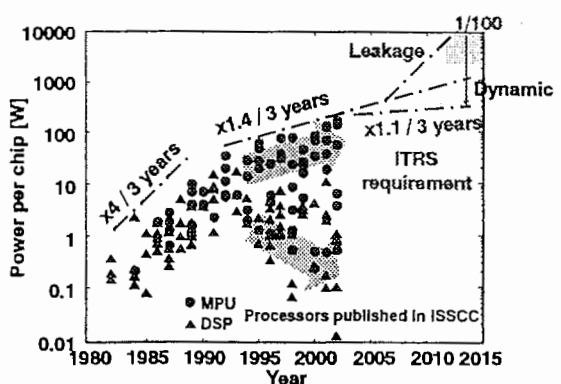
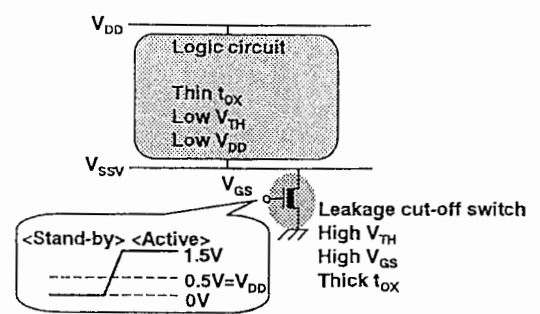


Fig.4 Trend in VLSI power consumption



Technology provides multiple kinds of MOSFET's and designers make use of the gift.

T. Inukai et al, CICC, May 2000

Fig.8 Stand-by leakage reduction through technology-circuit cooperation

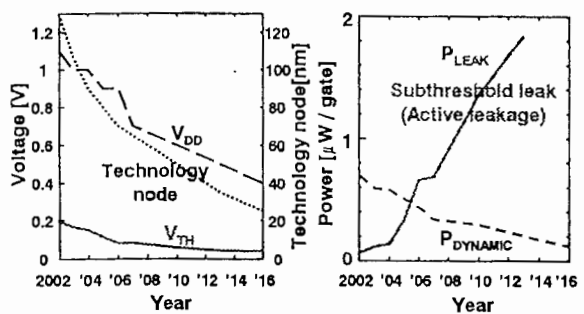
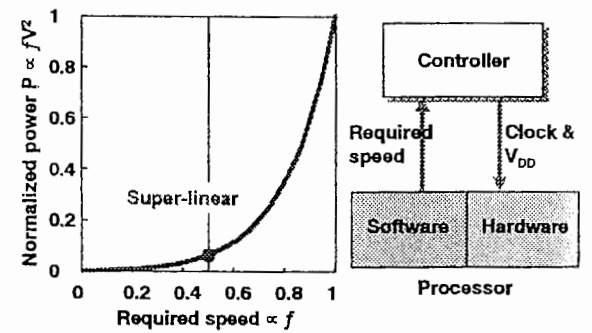


Fig.5 Active leakage makes things more challenging



If you don't need to hustle, relax and save power.

S.Lee, and T.Sakurai, "Run-Time Voltage Hopping for Low-Power Real-Time Systems", Proceedings of Design Automation Conference, pp.806-809, June 2000

Fig.9 Dynamic power reduction through software-hardware cooperation

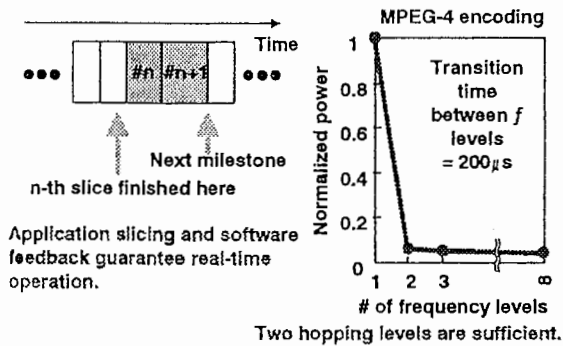
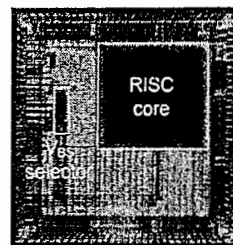
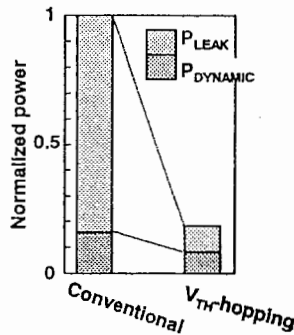


Fig.10 Applicable to real-time application VDD-hopping



$V_{DD}=0.5V$
 $V_{THlow}=0V$
 94% $f/2$ operation

V_{TH} is dynamically changed by means of back-gate bias.

K. Nose et al, JSSC, Mar. 2002

Fig.14 VTH-hopping saves 80% of active leakage



Fig.11 VDD-hopping with real-time O/S

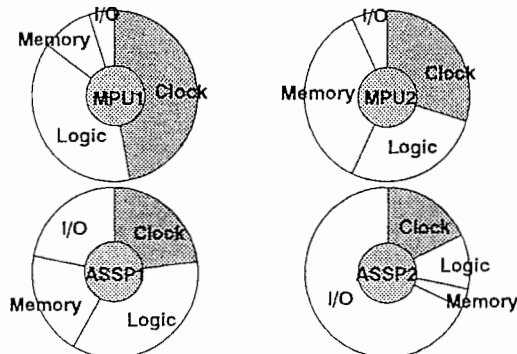


Fig.15 Power distribution is diverse

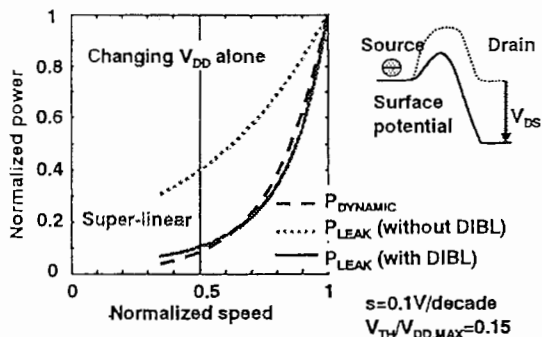
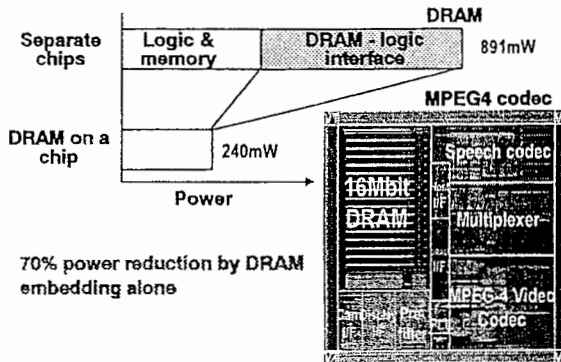


Fig.12 VDD-hopping reduces active leakage power with Drain Induced Barrier Lowering (DIBL)



Courtesy Toshiba, ISSCC 2000

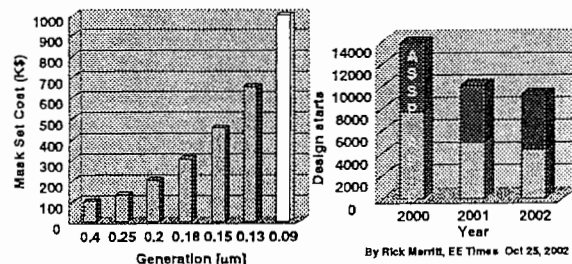
Fig.16 System-on-a-Chip reduces I/O power

LOGIC V_{DD} : Low (0.5V) V_{TH} : Low (0V) High-perf.	MEMORY V_{DD} : High (1V) V_{TH} : High (0.3V) Low-leakage
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• 0.5V 400MHz 16bit processor
 • 3.5mW

H.Kawaguchi, K.Kanda, K.Nose, S.Hattori, D.D.Antono, D.Yamada, T.Miyazaki, K.Inegaki, T.Hiramoto, and T.Sakurai, "A 0.5-V, 400-MHz, VDD-Hopping Processor with Zero-VTH FD-SOI Technology," ISSCC, pp.108-109, Feb. 2003.

Fig.13 Low-voltage, low-power VDD hopping processor



Source: Rahul Goyal, Intel - Nov 2001 SEMI Mtg

By Rick Merritt, EE Times, Oct 25, 2002

http://www.seetimes.com/printableArticle7doc_id=0E62002102550052

- ◆ NRE for a SoC is getting \$5M-10M and without over \$20M sales it is difficult to make a SoC. by Bryan Lawlis, Gartner Dataquest
- ◆ Number of design starts is declining from 1997.
- ◆ Overhead of power and area of FPGA, and software is 40 times of SoC.

Fig.17 Exploding Non-Recurring Engineering (NRE) cost

SoC	Cell based Memory embedding	Highest performance and power efficiency	Slow TAT (3M-1Y) Huge NRE High risk in development Still needs a few masks and semiconductor fab ASIC biz model (M for plants)
Quick CA	LightSpeed ChipExpress ISSP (NEC) VGPA (CMU)	QTAT (1W + 1M) Higher signal integrity	40 times more area and power and 3 times slower than SoC Still needs boards
FPGA	Xilinx Altera	QTAT (1day + 1M) Fully programmable in gates Established design env.	Killer applications? New design environments
Reconfigurable processor	DRP (NEC) iPFlax (Fujitsu Invested)	10 times more area efficient than FPGA	New design environments No gate level parallelism
Multi-lane processor	MeP (Toh'n'ba) MOZ (Mitsubishi)	Just need programs Multimedia oriented	New design environments Known good die
Advanced assembly	SIP Embedded Circuit Board	Good balance of QTAT (1M) and performance Combining tested chips Hybrid technology integration	No standardization of I/O

Fig.18 Contenders for lower NRE

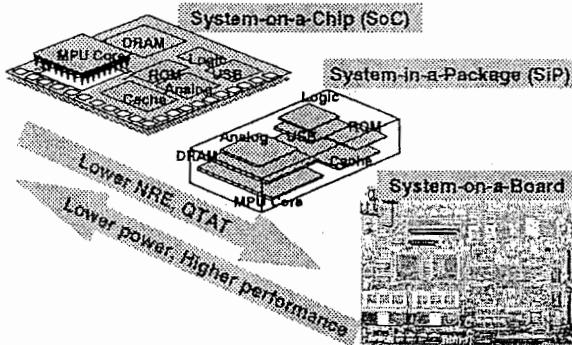
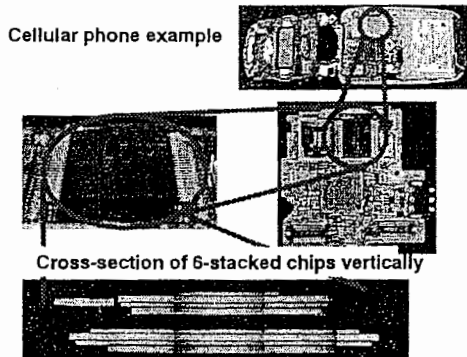
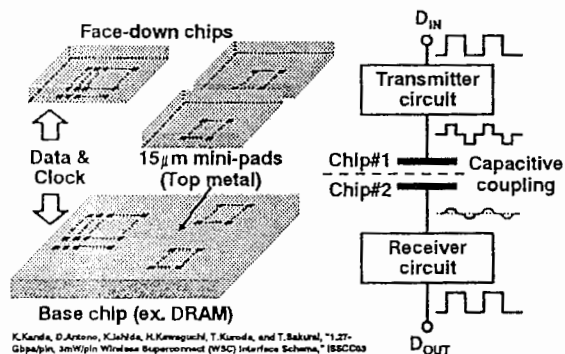


Fig.19 System-in-a-Package (SiP) will reduce NRE



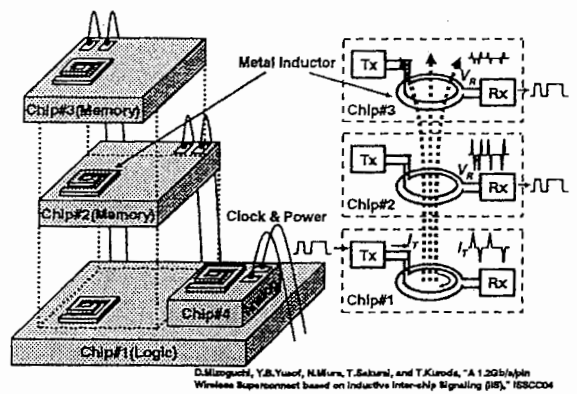
Courtesy North Corporation

Fig.20 System-in-a-Package has come to market



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Fig.21 Wireless Super-Connect achieving 1Tbps/mm²



D.Milman, Y.B.Yuof, N.Mil'man, T.Bakura, and T.Kuroda, "A 1.2Gb/s/in Wireless Superconnect based on Inductive Inter-Chip Signaling (IS)," ISSCC04

Fig.22 Inductive Wireless Super-Connect connecting multiple chips

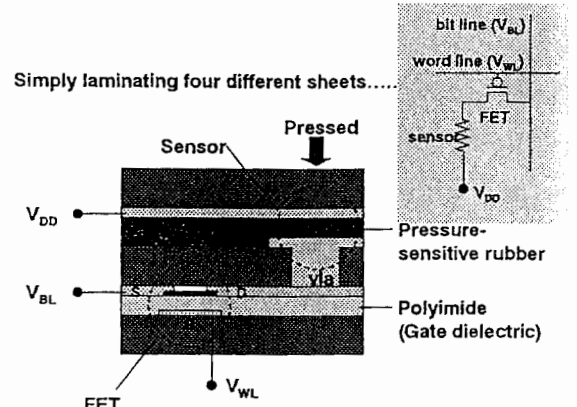


Fig.23 Integration of organic field-effect transistors and rubbery pressure sensors for artificial skin applications

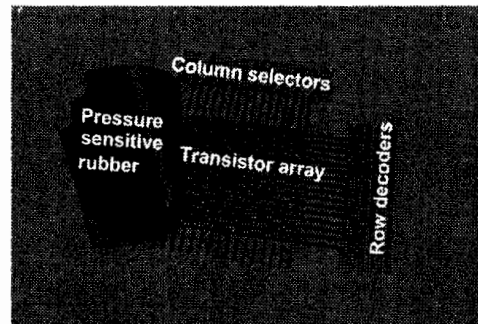
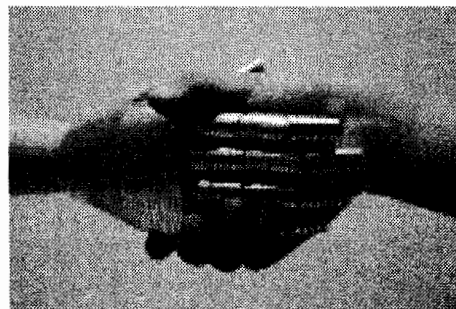


Fig.24 Cut-and-paste organic FET customized IC's application to artificial skin



Artificial skin may add low-power delicate touch sensing to robots