An LSI for V_{DD}-Hopping and MPEG4 System Based on the Chip

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ABSTRACT

An LSI is fabricated and measured to demonstrate the feasibility of the V_{DD}-hopping scheme in a system level. In the scheme, supply voltage, V_{DD}, is dynamically controlled through software depending on workload. The V_{DD}-hopping scheme is shown to reduce the power to less than 1/4 compared with the conventional fixed-V_{DD} scheme. The power saving is achieved without degrading the real-time feature of an MPEG4 system.

1. INTRODUCTION

High-performance and low-power features are pursed extensively in CMOS LSI designs to meet the increasing needs for portable processor systems such as palmtop PDA's and intelligent cellular phones. There have been several proposals to reduce the system power by changing supply voltage, V_{DD}, dynamically [1]-[6]. Redesign of a processor, however, is required to implement these proposals, and it is difficult to make use of off-the-shelf processors sold on the market which produces a big barrier to use the concept of the dynamic voltage scaling, DVS.

This paper presents a novel LSI and a system to realize the DVS, which can utilize off-the-shelf processors. The novel DVS is called V_{DD}-hopping. The V_{DD}-hopping utilizes dynamic adjustment of clock frequency, f, and V_{DD} depending on the workload of the processor [7][8]. When the workload is decreased, the power would be drastically reduced by decreasing f and V_{DD}. By reducing the number of discrete voltage levels used in the DVS, the V_{DD}-hopping make it possible to use off-the-shelf processors. The reduction of number of levels is crucial in a product because many test sequences should be run, if the number is large. This V_{DD}-hopping is applied for the first time to an MPEG4 multimedia system without degrading real-time feature of the system.

2. V_{DD}-HOPPING

Figure 1 shows three approaches to reduce power when the workload is 50%. The approach (A) and (B) are the conventional approach while (C) is the proposed V_{DD}-hopping, which shows the highest power saving as indicated in Fig. 2.

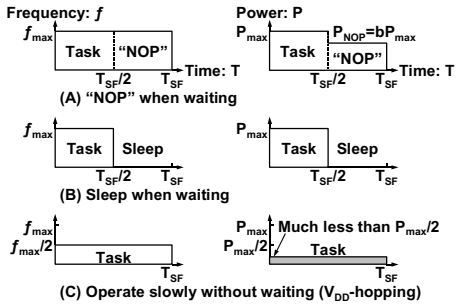

Fig. 1. Three approaches to reduce power when the workload is 50%. f_{max} is the maximum f when V_{DD} is at maximum, V_{DDmax}, and then, the maximum power, P_{max}, is consumed. V_{DD} is fixed to V_{DDmax} in (A) and (B), and only the task period is controlled. On the other hand, in (C), f and V_{DD} are controlled dynamically.

(A) "NOP" when waiting: Even if there is no task to be done, application programs and operating systems, OS, such as μITRON usually execute "NOP" loop to wait for either an interrupt or a next task. Then, clock generators with PLL/DLL, memories including caches and address calculations are executed which consume certain level of power, bP_{max}, where b is less than one. The normalized power, NP, is expressed as follows when the normalized workload is NW.

$$NP(NW) = (1-b)NW + b.$$

(B) Sleep when waiting: If a sleep mode is available on a target processor, application programs and OS may use the sleep mode after a task is completed until the next task starts. In this case, since usually almost no power is consumed in the sleep mode, NP is given as follows.

$$NP(NW) = NW.$$

(C) Work slowly without waiting (V_{DD}-hopping): This corresponds to the V_{DD}-hopping case. NW and NP are given by functions of V_{DD} with α-power law MOS model [9] as follows.

$$NW(V_{DD}) = \frac{V_{DD\,max}}{V_{DD}}\left(\frac{V_{DD}-V_{TH}}{V_{DD\,max}-V_{TH}}\right)^{\alpha},$$

$$NP(V_{DD}) = \left(\frac{V_{DD}}{V_{DD\,max}}\right)^{2} NW(V_{DD}),$$

$$NP(NW) = NW^{\frac{\alpha+1}{\alpha-1}} \quad if \quad V_{TH} = 0.$$

V_{TH} denotes the threshold voltage of MOSFET. α represents a velocity saturation index, and is about 1.2 in a recent short-channel MOSFET while 2.0 in a long-channel one (Shockley model). NP dependence on NW for the three cases is shown in Fig. 2. It is clear that the total power is decreased effectively with the DVS. Furthermore, it is seen from the figure, as MOSFET shrinks, and α decreases, the effectiveness of the V_{DD}-hopping increases. This is because, if α is small, since the speed dependence on V_{DD} is small, V_{DD} can be decreased more.

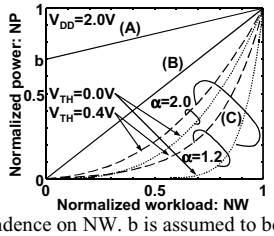

Fig. 2. NP dependence on NW. b is assumed to be 0.7.

The algorithm to adaptively change V_{DD} depending on the workload is of importance. Since the workload depends strongly on data, the control should be dynamic in run-time, and should not be static in a compile-time. It is too late to notice that the past task was an easy task which can be done much less than the worst-case execution time, WCET, because, once the task is completed, there is no way to change V_{DD} to lower the power. On the other hand, it is impossible to predict the workload of the task to be done in the future without error. To solve this problem, the algorithm introduces an application slicing and a software feedback loop. By chopping an application into slices, executing the first slices at V_{DDmax}, and checking the current time and the time margin to execute the next slice, the optimum V_{DD} is adaptively selected by a software

feedback loop. The details of the method used in this paper are summarized as follows with the help of Fig. 3.

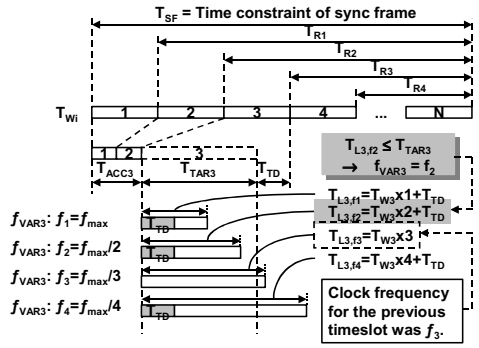

Fig. 3. Method to determine f and V_{DD}.

(A) A task is sliced into N timeslots. Following parameters are obtained through static analysis of an application program or direct measurement [10].

- T_{SF}: Time constraint of sync frame where sync frame is the maximum time allowed for the task.
- T_{Wi}: WCET of i-th timeslot
- T_{Ri}: WCET from (i+1)-th to N-th timeslot

(B) For each timeslot, the target execution time, T_{TARi}, is calculated as $T_{TARi}=T_{SF}-T_{ACCi}-T_{TD}-T_{Ri}$ where T_{ACCi} is execution time accumulated from 1st to (i-1)-th timeslot, and T_{TD} is a transition delay to change f and V_{DD}.

(C) For each candidate f_j, $f_j=f_{max}/j$ (j=1, 2, 3…), estimated maximum execution time, $T_{Li,fj}$, is calculated as $T_{Li,fj}=T_{wi}$ x j+T_{TD}. If f_j is equal to one of (i-1)-th timeslot, $T_{Li,fj}=T_{wi}$ x j.

(D) f of i-th timeslot, f_{VARi}, is determined as minimum f_j whose $T_{Li,fj}$ does not exceed T_{TARi}.

Thus, f and V_{DD} are dynamically controlled on a timeslot-by-timeslot basis inside each task by software. It should be noted that the proposed algorithm guarantees the real-time feature of the application. The relationship between f and V_{DD} is obtained by measurements.

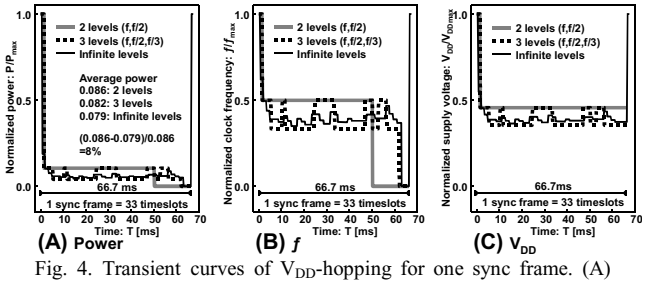

Fig. 4. Transient curves of V_{DD}-hopping for one sync frame. (A) Power. (B) f. (C) V_{DD}.

Figure 4 shows transient curves of power, f and V_{DD} obtained by a simulation for an MPEG4 SP@L1 codec with the V_{DD}-hopping for one sync frame. If more than two f levels, hence more than two V_{DD} levels are provided, more power reduction is possible, but the power improvement is 8%. Moreover, if more hopping levels are provided, there are test issues since speed test should be run at more levels than two. In the case of two hopping levels, f_{max} is used only 6% of the time while the processor run at $f_{max}/2$ for 70% of the time. For the rest of the time, the processor is in the sleep mode. f_{max} is still needed because the processor will run at f_{max} for 100% of the time, when worst-case data comes which is very unlikely, and for most of the time, the workload is about a half on average. This tendency holds for other applications such as MPEG2 decoding and VSELP voice codec which are also simulated, and about an order of magnitude improvement in the power are assured.

3. BREADBOARD DESIGN

An MPEG4 codec system is built to demonstrate the feasibility of the V_{DD}-hopping as shown in Fig. 5. The system makes use of the off-the-shelf processor, Hitachi's SH-4, and its embedded system board [11][12]. A block diagram of the V_{DD}-hopping system is shown in Fig. 6. H.263 standard image sequence "carphone" is used as input data. The image is stored in the flash ROM as raw data.

The optimum f and V_{DD} are calculated by the processor with the V_{DD}-hopping algorithm described above. Then the information is sent through I/O bus of the processor and to VME bus, which controls V_{DD}-hopping board implemented by an FPGA, Altera EPM7064. Because only I/O instructions are required to implement the V_{DD}-hopping, no new instruction set is needed. This makes it possible to implement the V_{DD}-hopping system without redesigning the processor itself.

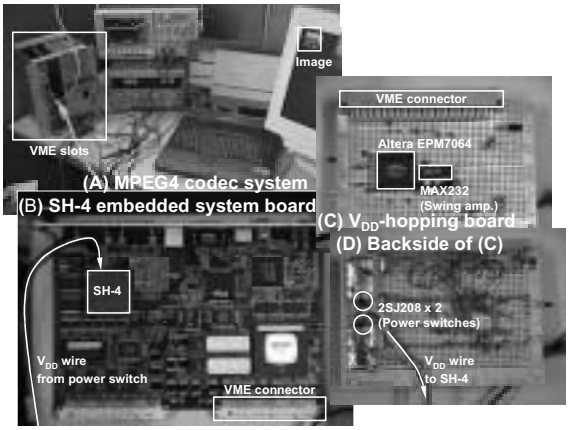

Fig. 5. (A) MPEG4 codec system with V_{DD}-hopping. (B) SH-4 embedded system board. (C) V_{DD}-hopping board. (D) Backside of (C).

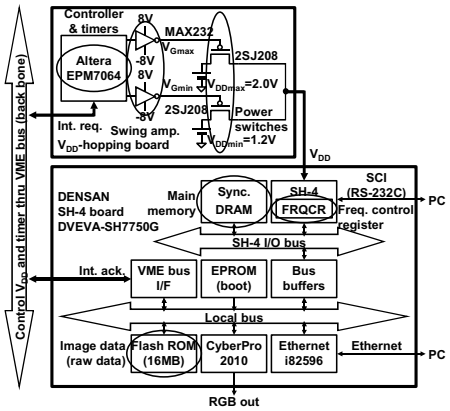

Fig. 6. Block diagram of V_{DD}-hopping system.

The FPGA has timers in it. One of the timers watches the execution time, tells the current time to the processor when asked through the VME bus, is set when the processor goes into a sleep mode, and wakes up the processor with an interrupt signal when the preset time comes. This is needed because no one would wake up the processor, once the processor goes into the sleep mode unless the timer in the FPGA triggers the wake-up process. Since no special functions of the processor are used, the proposed method of implementing the V_{DD}-hopping can be applied to any processor.

There are a couple of points which should be handled with care in implementing the board level V_{DD}-hopping. The following sections describe these points.

3.1 Power Switch

On the V_{DD}-hopping board, V_{DD} is hopped between V_{DDmax} and V_{DDmin} by power switch MOSFET's (2SJ208 x 2), which has one of the lowest threshold voltages on the market. The threshold voltage, however, is 2.8V, which is higher than the V_{DD} specification of the processor, 2V. Then, the MOSFET never turns on as it is. In Fig. 6, RS-232C driver, MAX232 is used as a voltage swing amplifier that amplifies the signal to ±8V. In this V_{DD}-hopping system, the number of the power switches is limited to two. The numbers can be increased but the area overhead is also increased.

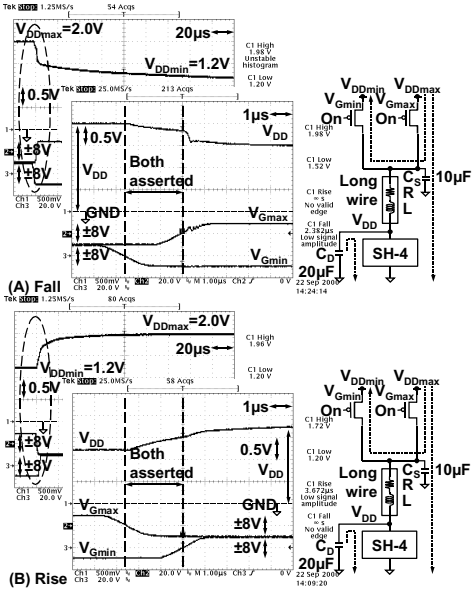

Fig. 7. V_{DD} waveforms when there is a period while both V_{Gmax} and V_{Gmin} are asserted. (A) V_{DD} falling from V_{DDmax} to V_{DDmin}. (B) V_{DD} rising from V_{DDmin} to V_{DDmax}.

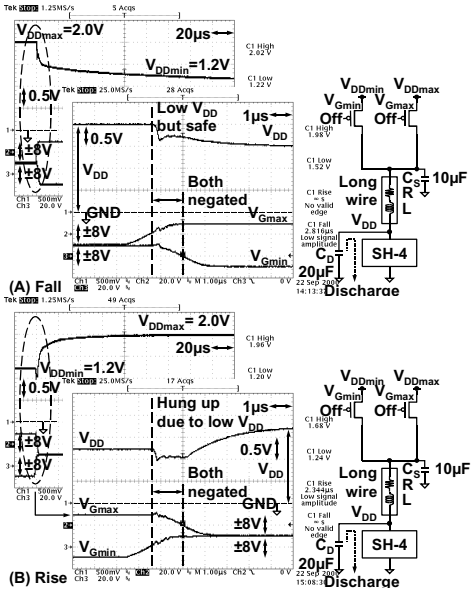

Fig. 8. V_{DD} waveforms when there is a period while both V_{Gmax} and V_{Gmin} are negated. (A) V_{DD} falling from V_{DDmax} to V_{DDmin}. (B) V_{DD} rising from V_{DDmin} to V_{DDmax}.

Figures 7 and 8 are measured V_{DD} waveforms. The measured fall and rise time of V_{DD} are less than 200µs and 100µs respectively with a decoupling capacitance at the node V_{DD}, C_D+C_S, of 30µF.

A care should be taken for the overlap of the V_{DDmax} enable signal, V_{Gmax}, and of the V_{DDmin} enable signal, V_{Gmin}. In switching between V_{DDmax} and V_{DDmin}, there are two cases: One is when there is an overlap between the signals, and the other case is when there is no overlap between the signals. It is eventually impossible to turn on one MOSFET and turn off the other MOSFET exactly at the same time. If there is an overlap whose situation is depicted in Fig. 7, large current may flow from V_{DDmax} to V_{DDmin} which may cause a problem. However, thanks to the decoupling capacitance C_D, no spike-like noise nor voltage drop are observed. The overlap between the signals is set to 2µs.

If there is no overlap, there is a period while V_{DD} line is completely cut off from both V_{DDmax} and V_{DDmin} which may cause a problem. This is really a problem as seen in Fig. 8. V_{DD} sags below V_{DDmin}, which may put the system in hung-up. In conclusion, the switching between V_{DDmax} and V_{DDmin} should be carried out with the period while both V_{DDmax} and V_{DDmin} are connected to V_{DD} line for a short time.

One more care other than the timing overlap is for a power-on sequence. At power-on, V_{Gmax} should be asserted to connect the highest V_{DD}, V_{DDmax}, to V_{DD} line at boot-up process.

3.2 Clock Frequency

The processor has a clock frequency control register, FRQCR, as shown in Fig. 6. The FRQCR can change the internal clock frequency instantaneously. The internal clock frequency is synchronized with external clock of 33MHz. Since only 100MHz and 200MHz whose ratio is an integer are used as the clock frequencies, there is eventually no synchronization problem at the interface of the processor with the external systems. In a general processor, the clock frequency control register might not be implemented, and at that time, two or more frequencies should be applied by the V_{DD}-hopping controller. An LSI implementation described afterwards output frequencies by itself.

3.3 Power

Figure 9 shows the measured power characteristics of the V_{DD}-hopping system. The power of the processor at 200MHz is 0.8W while the power at 100MHz is 0.16W. The power in the sleep mode is 0.07W. Since the average time to use 200MHz is 8%, that to use 100MHz is 86%, and that for the sleep mode is 6%, the average power is 0.21W which should be compared with 0.8W without the proposed V_{DD}-hopping. The processor used in this system is not optimized for the very low- voltage operation. If the processor has been designed carefully, the V_{DDmin} could be below 0.9V instead of 1.2V. In this case, the power could be reduced to about a half.

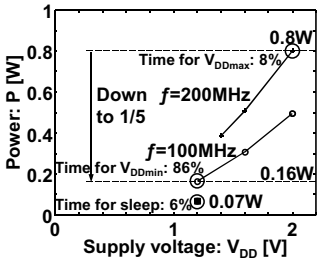

Fig. 9. Measured power characteristics of V_{DD}-hopping system.

4. LSI DESIGN

Encouraged by the success in the breadboard system, a V_{DD}-hopping LSI is designed and fabricated which has the function describes in the previous chapter. Fundamentally, the FPGA portion of the system is implemented by an LSI based on a standard cell design style.

The gate width of the power switch is critical in the design. The simulated V_{DS} curve is shown in Fig. 10. In the process technology used for the LSI design, the threshold voltage is 0.6V which is smaller than V_{DDmin}, 1.2V, so that the signal swing amplifier is not needed which was

required for the breadboard design. The gate width of 270,000μm is found to be appropriate if the voltage drop by the switch is set to be less than 0.05V. This gate width also draws sufficiently large current of 0.4A through it if V_{DD} is V_{DDmax}, 2.0V.

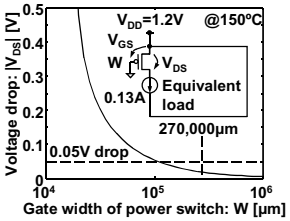

Fig. 10. Voltage drop dependence on gate width of power switch. This shows the worst case because of the minimum gate bias, V_{GS}.

Figure 11 shows a schematic diagram of the V_{DD}-hopping LSI. As described in the previous chapter, the timing overlap between V_{Gmax} and V_{Gmin} is critical. In order to adjust the period of the overlap, a programmable timer is put at the gate of the power switch. The LSI also has an all-purpose decoder, a clock frequency selector to select either f_{max} or $f_{max}/2$, and timers with the interruption signal to watch the execution time and trigger the wake-up process. The clock frequency selector can output only f_{max} and $f_{max}/2$. In general, a processor must be halted while f and V_{DD} is being changed to eliminate malfunctions due to the transition.

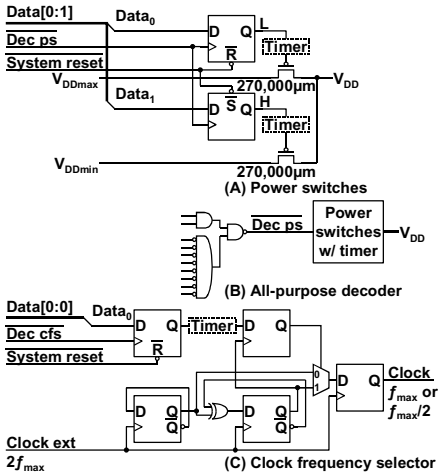

Fig. 11. (A) Power switches. Programmable timers adjust the timing overlap. (B) All-purpose decoder. (C) Clock frequency selector. Programmable timer avoids f changing during a program execution.

Figure 12 shows the measured waveforms of V_{DD} and the sleep signal of the processor. It should be noted that just two sync frames are shown in the figure. It is seen from the figure that V_{DDmax} is used only 8% of the time. The normalized workload is 51% (8% x 1+86% x 0.5+6% x 0).

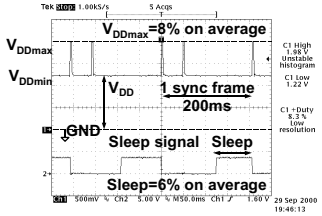

Fig. 12. Measured waveforms of V_{DD} and sleep signal of the processor. They are similar to the two level case of Fig. 4.

Figure 13 shows a power comparison between the V_{DD}-hopping and other fixed-V_{DD} schemes for the MPEG4 codec. V_{DD}-hopping scheme is measured to consume 0.21W, and can reduce the power to less than 1/4 of the fixed-V_{DD} scheme.

The LSI has been fabricated with a 0.6μm triple metal CMOS technology. The LSI looks like Fig. 14 and consumes 0.01W when the external clock is 33MHz. The size is about 4.6mm x 2.3mm including two power switches.

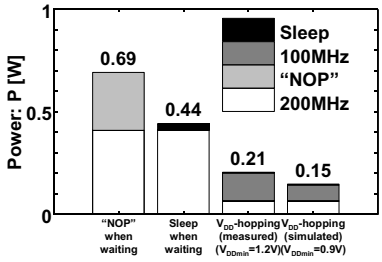

Fig. 13. Power comparison between V_{DD}-hopping and fixed-V_{DD} schemes.

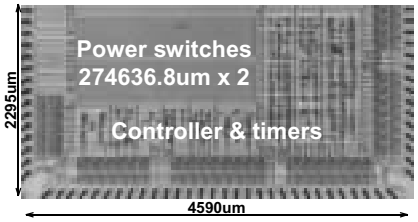

Fig. 14. LSI for V_{DD}-hopping.

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