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# Current Sensing Device for Micro-IDDQ Test

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## SUMMARY

In LSIs with more than 1 million gates, detection of the defective locations becomes difficult. In particular, in the case of an abnormality in the standby current, excessive power is consumed even if operation is successful. Hence, it is necessary to identify the error location in order to reduce power consumption. The IDDQ test detects the error by measuring the static current in standby for each circuit block. A typical implementation is the BICS (Built-In Current Sensor). However, the conventional method has the problems of reduction of the noise margin and degradation of the circuit speed. In this paper, two types of current sensors, the Lorentz force MOSFET (LMOS) and Hall effect MOSFET (HEMOS), based on a magnetic sensor circuit using CMOS technology, are proposed. These sensors are capable of non-contacting and non-disturbing current measurement. A circuit for applications to the IDDQ test is described. © 2001 Scripta Technica, Electron Comm Jpn Pt 2, 84(9): 21–27, 2001

**Key words:** IDDQ test; Hall effect; current sensor; low power consumption.

## 1. Introduction

Recently, LSIs integrating more than 1 million gates have become a reality. The number of gates on one chip is expected to increase in the future. As the number of gates is increased, the detection of defective locations becomes difficult. In particular, the abnormal standby current and microshorts dependent on the layout pattern cause consumption of excessive power even if the circuit is operational. It is difficult to detect these abnormal standby current because they are not errors on the layout, unlike leak anomalies due to design error. In addition, statistical analysis is indispensable for identification of these defects, so that measurement of many chips is needed. For detection of abnormal current, methods employing infrared are widely used. Specialized equipment is needed and the measurement time may be problematic. Hence, it is important to the development of low-power LSI to develop an IDDQ test circuit that can measure the current of the power supply lines on the chip at a practical speed.

The IDDQ test detects the abnormal standby current by measuring the standby current for each circuit block. A typical implementation is the BICS (Built-In Current Sensor) [1, 2] as shown in Fig. 1. A BICS circuit is cascade-connected to the circuit to be measured so as to detect when more than a certain amount of current flows. In this method, however, there are problems of reduction of the noise margin and circuit speed due to the fact that the potential of the VGND deviates from the GND potential (as the potential of VGND changes depending on the operation state).

It is also necessary to detect where the cause of the abnormal standby current occurs in more than 1 million gates by using a measurement pad. On the other hand, the micro IDDQ test, in which the chip is divided into many circuit blocks and an IDDQ test is carried out for each block, will become more important in the future.

This paper proposes two types of current sensors, the Lorentz force MOSFET and the Hall effect MOSFET, that can carry out non-contacting and non-disturbing measure-

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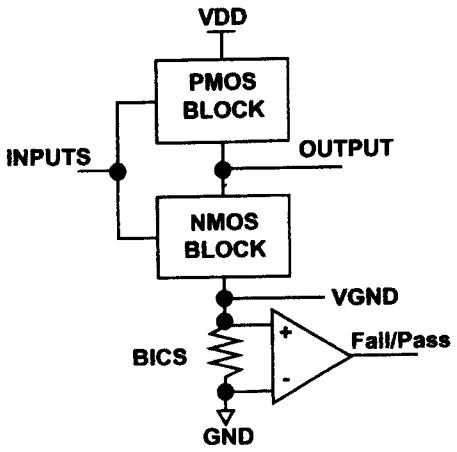


Fig. 1. Built-in current sensor circuit.

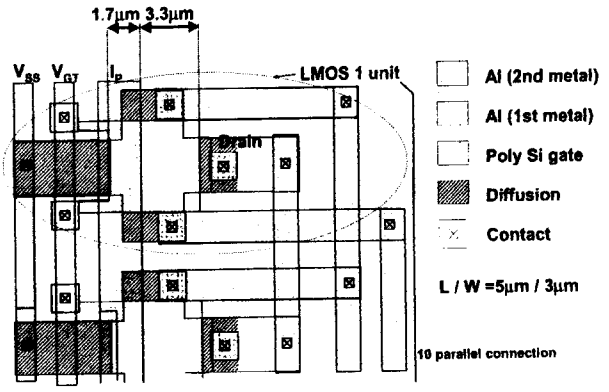


Fig. 3. Layout of LMOS.

ment based on CMOS technology, and describes the circuit to be applied for micro-IDDQ tests.

## 2. Current Sensor Using Lorentz Force (Lorentz Force MOSFET: LMOS)

### 2.1. Overview of LMOS

The structure of the LMOS is shown in Fig. 2. When the current $I_P$ flows in the power supply line to be measured, a magnetic field $B$ proportional to $I_P$ is generated around the line. When a transistor is placed under the power supply line, the electrons in the channel receive a Lorentz force as a result of the magnetic field $B$. Therefore, by means of the Hall effect [5], a voltage difference proportional to $B$ appears between Vo1 and Vo2. By measuring this voltage difference between Vo1 and Vo2, the current $I_P$ in the power supply line can be determined.

### 2.2. Layout and design of LMOS

Figure 3 shows the layout of the LMOS. Here, 10 LMOS are connected in parallel to average out the voltage difference so that the effect of fluctuations of the transistors within the chip is reduced. The channel length is the maximum possible in design so that the short channel effect and the fluctuations are alleviated. In this study, the overlap width of the gate and the power supply line is set to constant (1.7 μm) and the dependence on the width of the power supply line is studied.

Figure 4 shows a microphotograph of the fabricated chip using the conventional 0.5-μm two-layer CMOS process.

For the measurement of this chip, the circuit in Fig. 5 is used. The current value $I_P$ of the power supply line is derived by measuring the voltage difference $\Delta V_D$ of Vo1 and Vo2. Then, due to the effect of the $V_{DDT}$ line and GND line as well as the effect of the earth's magnetic field, $\Delta V_D$ is

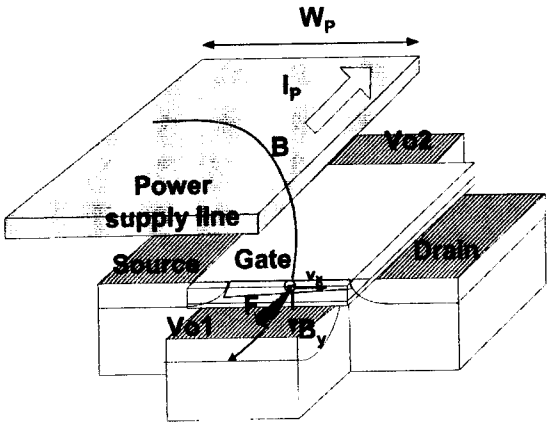


Fig. 2. Structure of LMOS.

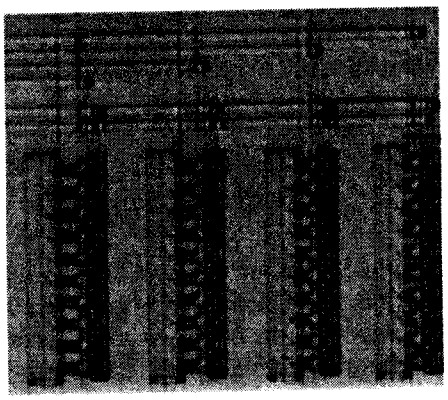

Fig. 4. Microphotograph of LMOS.

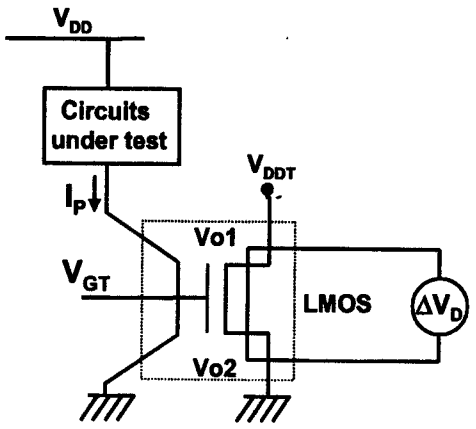


Fig. 5. Test circuit to measure the current of power supply line using LMOS.

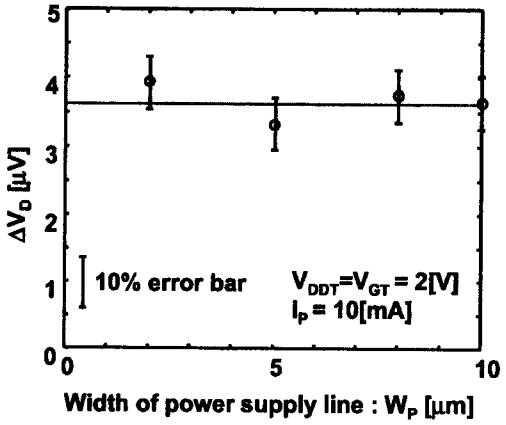


Fig. 7. Measured results for $\Delta V_D$ dependence on the width of power supply line.

generated even if the current $I_P$ of the power supply line is 0. However, the magnetic field generated by these effects is constant regardless of the value of $I_P$. It is therefore possible to eliminate these effects by taking the difference between $\Delta V_D$ with current in the power supply line and the corresponding value without current.

### 2.3. Measured results of LMOS

Figure 6 shows the relationship between the measured voltage difference $\Delta V_D$ of the LMOS and the current $I_P$ in the power supply line. At each measurement point, $\Delta V_D$ is proportional to $I_P$ if an error of 10% (which is estimated due to the very small voltage measurement, on the order of microvolts) is taken into account. Hence, $I_P$ is determined by measurement of $\Delta V_D$.

Figure 7 shows the dependence of $\Delta V_D$ on the line width ($W_P$) of the power supply line under measurement. It is found that $\Delta V_D$ is within the range of $\Delta V_D = 3.6\ \mu V \pm 10\%$. Hence, $\Delta V_D$ is almost constant regardless of $W_P$.

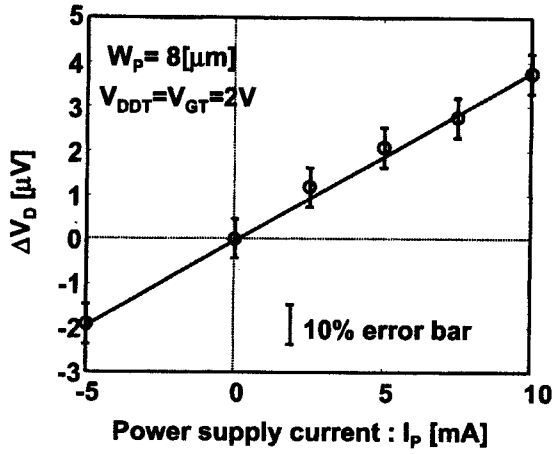


Fig. 6. Measured result for $\Delta V_D$ dependence on the current under test.

## 3. Current Sensor Using Split-Drain Structure (HEMOS)

### 3.1. Overview of HEMOS

In the previous section the effectiveness of LMOS as a current sensor was presented. However, when a current of 10 mA in a power supply line is detected, sensitivity is a problem, since the value of $\Delta V_D$ is extremely small, not exceeding a few microvolts. In this case the HEMOS (Hall effect MOSFET) is proposed as a device with higher sensitivity.

The structure of HEMOS is shown in Fig. 8. The operating principle is as follows. The Lorentz force due to the magnetic field $B$ generated by the current in the power supply line deflects the electron trajectories of the electrons in the HEMOS channel. Since the drain of the HEMOS is divided into two, the numbers of electrons entering Drains 1 and 2 are different when the electron trajectory changes. This difference causes a difference in currents in Drains 1 and 2. Since the difference depends on the Lorentz force, the current flowing in the power supply line can be measured if this current difference is detected.

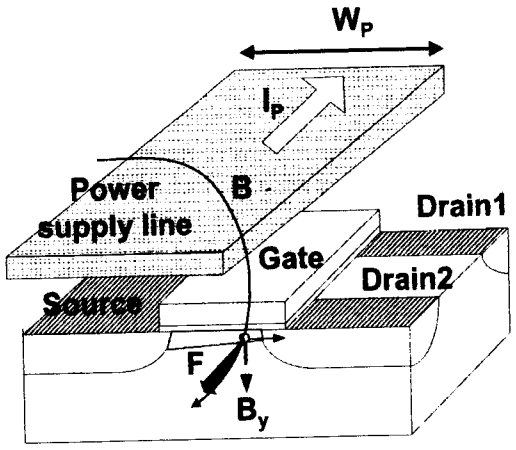


Fig. 8. Structure of HEMOS.

### 3.2. Layout and design of HEMOS

Figures 9 and 10 show the chip layout and microphotograph. This is designed with the 0.5-μm rule and two-layer interconnects. The current flow in the interconnect (power supply line) with a width of 50 μm placed on the first metal is detected. Figure 11 shows the measurement circuit. Identical external resistors are attached to Drains 1 and 2 so that the current is converted to a voltage. In this case, the difference between the resistors must be taken into account. Let the difference of two resistors be $\Delta R = R_2 - R_1$ and the currents in Drains 1 and 2 be $I_1$ and $I_2$ when the current $I_P$ flows in the power supply line. Then, $V_D$ is

$$V_D = I_1 R_1 - I_2 R_2$$

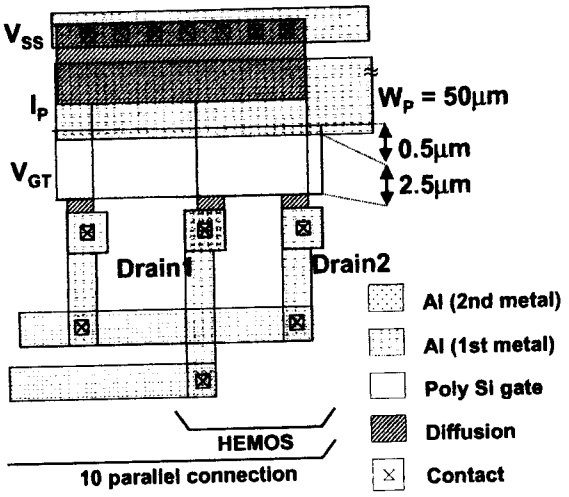


Fig. 9. Layout of HEMOS.

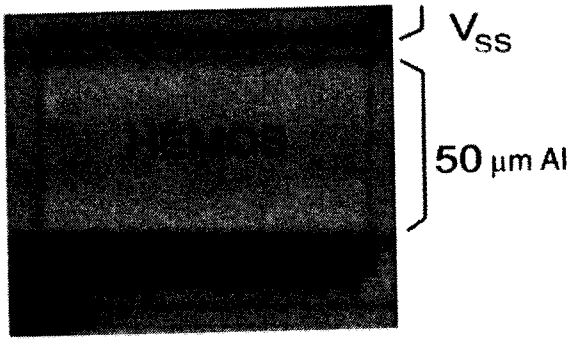


Fig. 10. Microphotograph of HEMOS.

$$= (I_{10}R_1 - I_{20}R_2) + (\Delta I_1 - \Delta I_2)R_1 - \Delta I_2 \Delta R \quad (1)$$

where

$$I_1 = I_{10} + \Delta I_1, \quad I_2 = I_{20} + \Delta I_2, \quad (2)$$

$$\Delta R = R_2 - R_1 \quad (3)$$

Here, $I_{10}$ and $I_{20}$ are the current in Drains 1 and 2 when there is no current in the power supply line, namely, $I_P = 0$. $\Delta I_1$ and $\Delta I_2$ are the changes of the currents in Drains 1 and 2 when the current in the power supply line changes from 0 to $I_P$. If $V_D$ in the absence of $I_P$ in the power supply line is $V_{D0}$, then

$$V_{D0} = I_{10}R_1 - I_{20}R_2 \quad (4)$$

Let us consider the difference $\Delta V_D$ between $V_D$ with a current flow in the power supply line and $V_{D0}$ without a current flow. Since $\Delta R << R_1$, the approximation

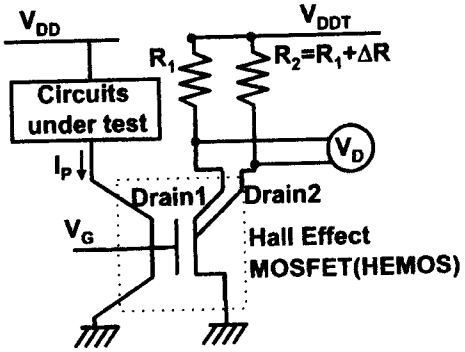


Fig. 11. Test circuit of HEMOS.

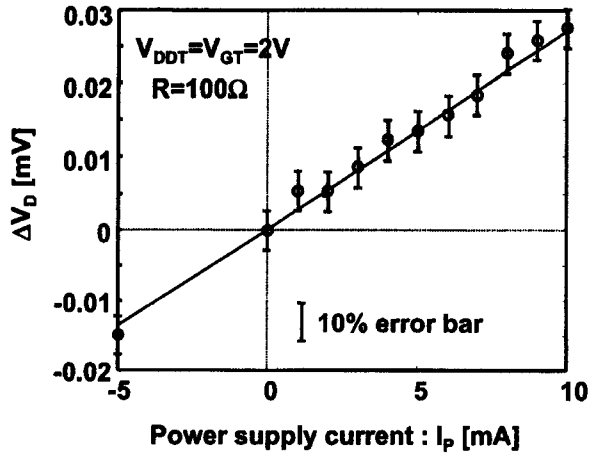


Fig. 12. Measured results for $\Delta V_D$ dependence on the current of the power supply line, $I_P$.

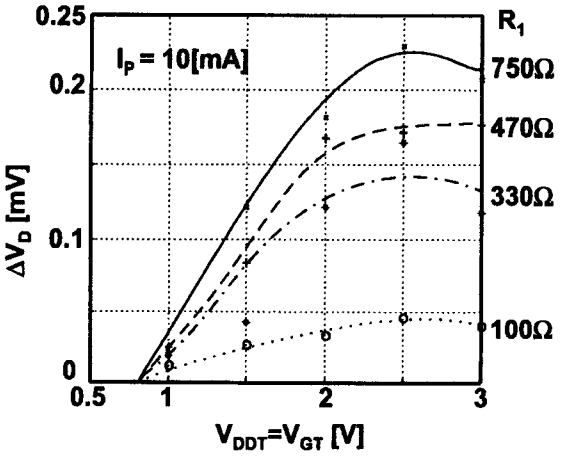


Fig. 14. Measured results for $\Delta V_D$ dependence on supply voltage of HEMOS.

$$\Delta V_D = V_D - V_{D0} \cong (\Delta I_1 - \Delta I_2)R_1 \qquad (5)$$

can be used. Therefore, $V_D$ becomes a function not dependent on $\Delta R$ or the corresponding current difference $(I_{10} - I_{20})$ and is proportional to the difference $(\Delta I_1 - \Delta I_2)$ of the current variations in Drains 1 and 2.

### 3.3. Measured results of HEMOS

Figure 12 shows the measured results of the relationship between the current $I_P$ of the power supply line and $\Delta V_D$ in the HEMOS. It is seen that $I_P$ is proportional to $\Delta V_D$ within an error of 10% as in the case of LMOS. Hence,

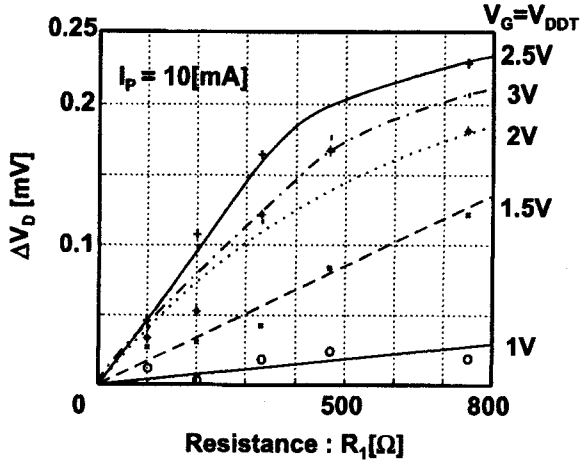


Fig. 13. Measured results for $\Delta V_D$ dependence on $R_1$.

similar to LMOS, $I_P$ is uniquely determined from the value of $\Delta V_D$.

Figures 13 and 14 show the relationships between $\Delta V_D$ and the external resistor $(R_1)$ used in the measurement circuit, and between $\Delta V_D$ and the power supply voltage $(V_{DDT})$ of the measurement circuit. When the external resistor and the drain voltage $V_{DDT}$ are large, the voltage drop across the external resistor is also large (e.g., the drop is about 0.3 V when $V_{GT} = V_{DDT}$ = 2 V and $R_1$ = 500 Ω). Therefore, $\Delta V_D$ is not proportional to the resistor value but converges. Also, in regard to $V_{DDT}$, there exists an optimum value as for LMOS. This optimum value is determined by nonuniformity of the drift velocity and surface charge density in the channel and also of the Lorentz force to the electrons in the channel due to the effect of the depletion region. In comparison to LMOS near the optimum point, the sensitivity $(\Delta V_D)$ of the HEMOS is about 0.2 mV as opposed to about 4 μV in the LMOS, and is thus improved by two orders of magnitude.

## 4. Micro-IDDQ Test Circuit

One of the important problems in the IDDQ test is the restriction of the number of pads in the test circuit. Usually, only a few pads are given for the test circuit. Hence, it is necessary to carry out an enormous number of current measurements with a limited number of pads. In order to overcome this problem, a method is proposed in which the current values of many power supply lines are measured with several pads by controlling the gate voltage of the LMOS and HEMOS.

Figures 15 and 16 show the micro-IDDQ test circuits using LMOS and HEMOS. A microphotograph of the

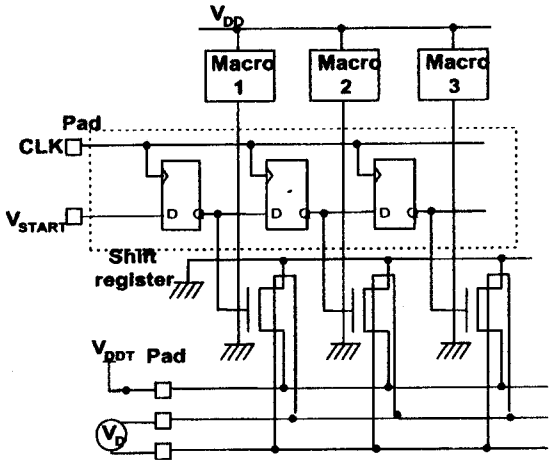


Fig. 15. Circuit diagram for the micro-IDDQ test by sharing pads among LMOSs.

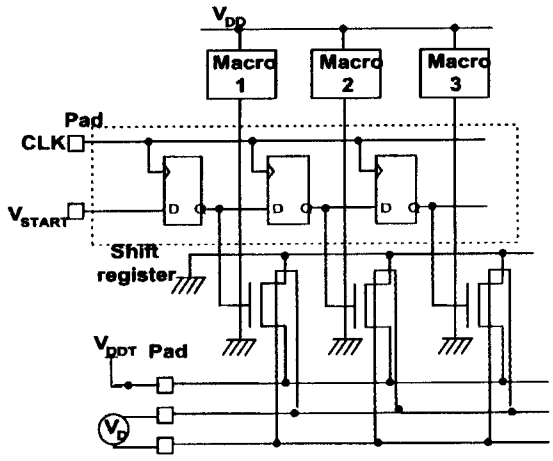


Fig. 16. Circuit diagram for the micro-IDDQ test by sharing pads among HEMOSs.

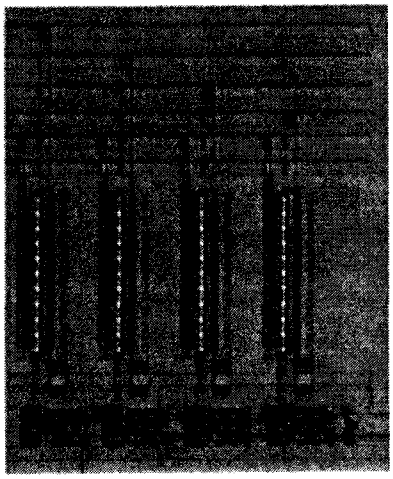

Fig. 17. Microphotograph of micro-IDDQ test using HEMOS.

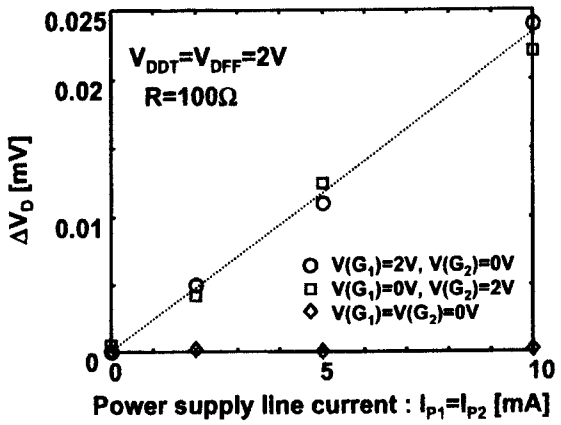


Fig. 18. Measured results of micro-IDDQ test circuit.

micro-IDDQ test circuit is shown in Fig. 17. Here, the case of HEMOS is presented. By means of a shift register, one of the HEMOS gates is set High while the remainders are Low. In the present MOSFET, the ratio of the drain currents with the gate at High and Low is about $10^6$. As shown in Fig. 14, $\Delta V_D$ of the HEMOS with its gate above the threshold value is sufficiently larger than $\Delta V_D$ of the HEMOS with its gate below the threshold value. Hence, the current flow in the power supply line of the HEMOS with its gate at High can be measured. The circuit in Fig. 16 is used for measurement of the HEMOS. The results are shown in Fig. 18. [Here, $V(G_1)$ and $V(G_2)$ are the HEMOS gate voltages for measurement of Macro1 and Macro2 while $I_{P1}$ and $I_{P2}$ are the currents of Macro1 and Macro2.] It is found that the currents of several power supply lines can be measured with this method. Since $\Delta V_D$ for the gate at Low is below the order of nanovolts (at an undetectable noise level), $\Delta V_D$ of the HEMOS with its gate at High can be measured accurately.

## 5. Conclusions

LMOS and HEMOS current measurement devices were fabricated for IDDQ test. It has been shown that the current in the power supply line can be measured in a non-contacting and non-disturbing manner. Micro-IDDQ test circuits were proposed and tested, confirming their operation. Using these devices, it is possible to detect abnormal currents accurately with a limited number of pads and to contribute to low-power design.

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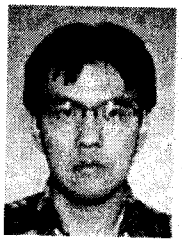

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