Variable Threshold Voltage CMOS in Series Connected Circuits

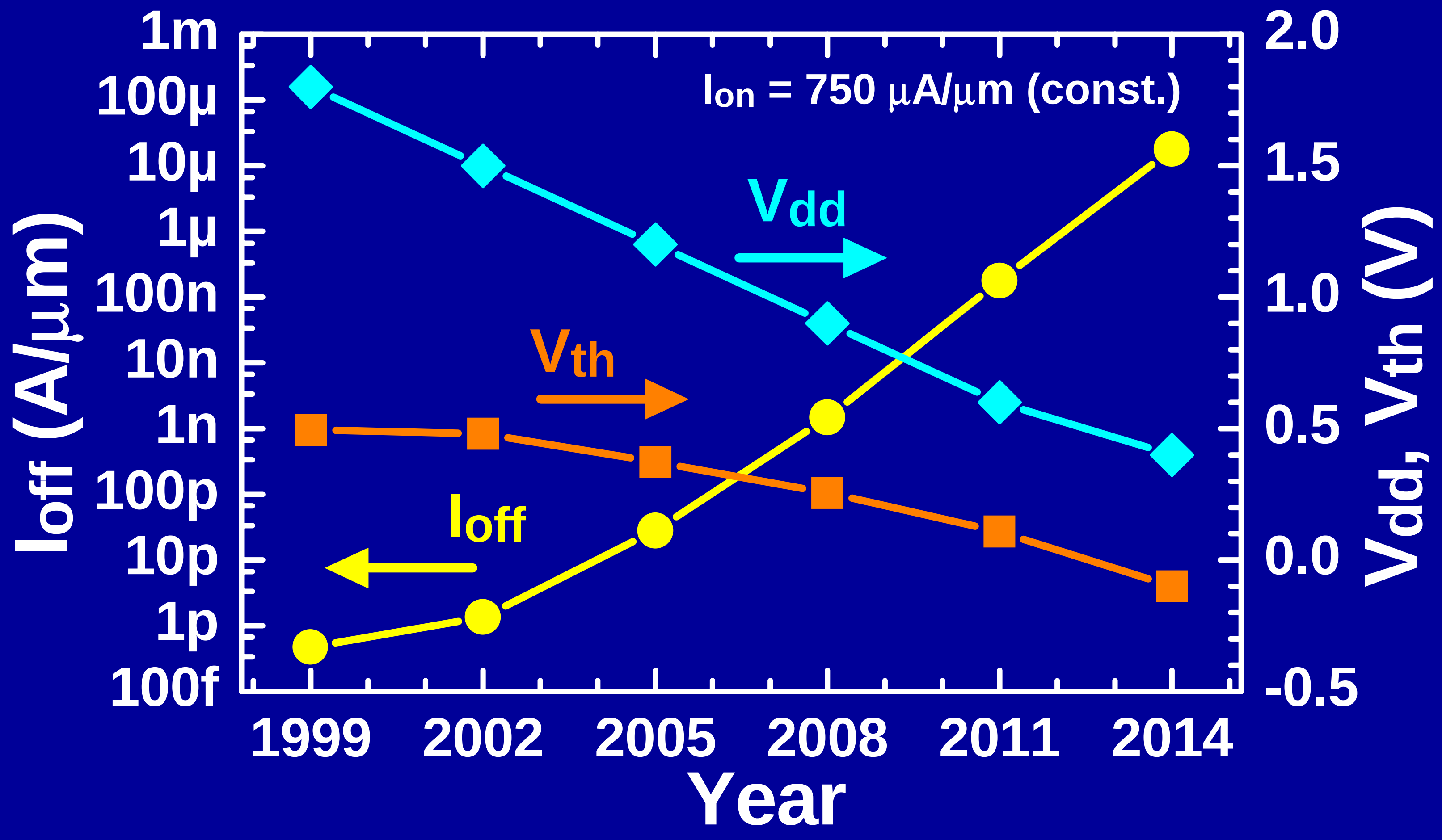
T. Inukai, T. Hiramoto and T. Sakurai

Institute of Industrial Science,
the University of Tokyo, Japan

Outline

- Background and objective
- Body effect factor and its relationship with device characteristics
- Device design in VTCMOS
  - Single devices
  - Series connected circuits
- Effect of velocity saturation
- Summary

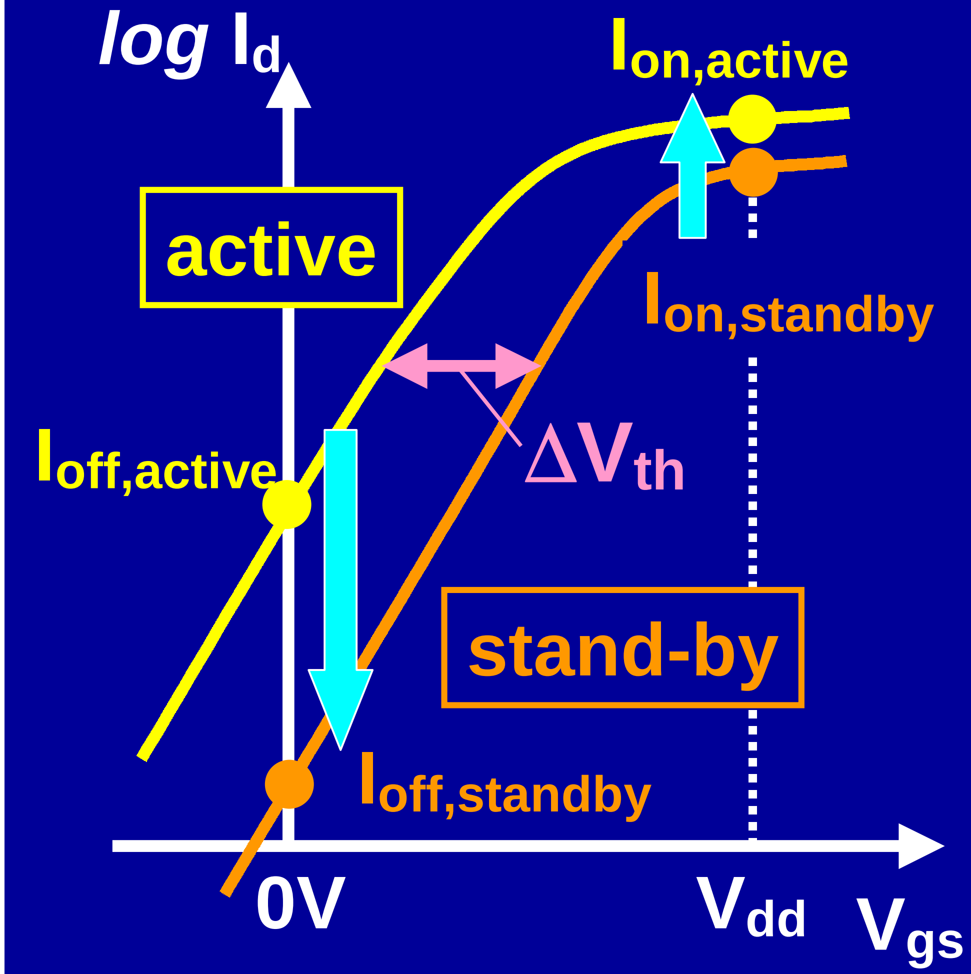
Explosion of Stand-by Power



Scaling of V_{th} with V_{dd} causes an increase of off-current.

➡ **Circuits with single (or fixed) V_{th} will fail due to explosion of stand-by power consumption.**

Variable Threshold Voltage CMOS



Utilizing the body effect,
V_{th} is controlled by V_{bs}.

Low V_{th} @ Active mode
→ enhancement of I_{on}
↕
High V_{th} @ Standby mode
→ suppression of I_{off}

What determines ΔV_{th}?

[ref.] T. Kuroda *et al*. IEEE JSSC, 31, 1770 (1996).

Objective

- **Investigation of optimum device design in variable threshold voltage CMOS (VTCMOS) by means of device simulation from the viewpoints of**
  - **Device performance (single device)**
  - **Circuit performance (series connected circuit)**

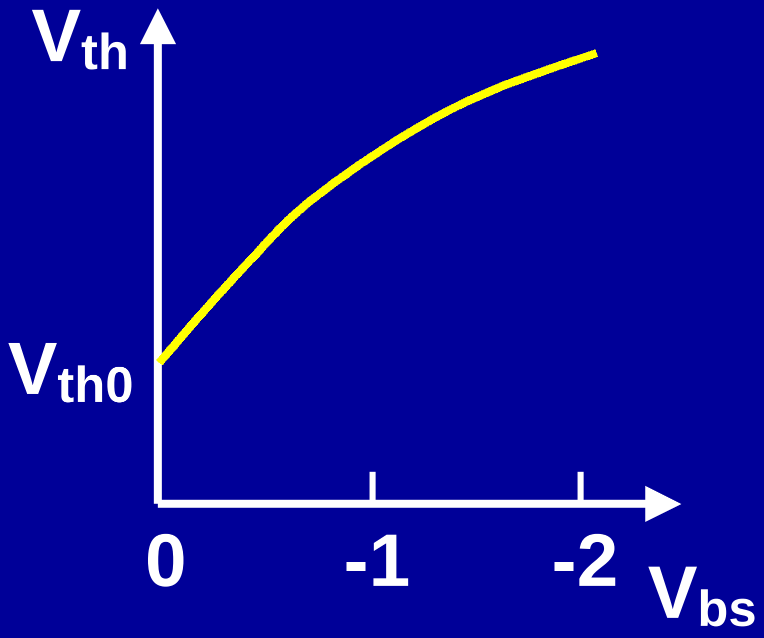
↓

Guideline for device design in VTCMOS

Outline

- Background and objective
- **Body effect factor and its relationship with device characteristics**
- Device design in VTCMOS
  - Single devices
  - Series connected circuits
- Effect of velocity saturation
- Summary

Body Effect Factor



V_{th} is varied by the body effect

$$V_{th} = 2\phi_F + \frac{\sqrt{2q\varepsilon N_a(2\phi_F + |V_{bs}|)}}{C_{ox}}$$

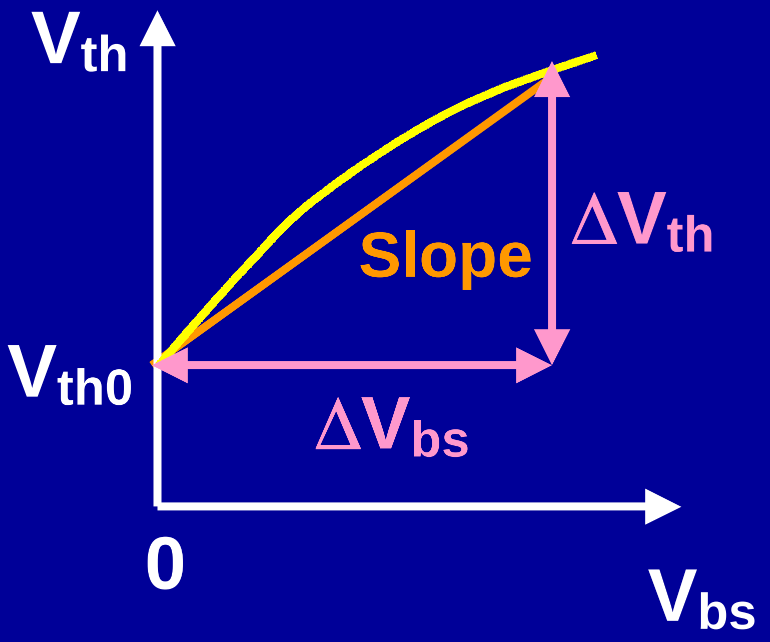
$$\Delta V_{th} = \frac{\sqrt{2q\varepsilon N_a}}{C_{ox}}\left(\sqrt{2\phi_F + |V_{bs}|} - \sqrt{2\phi_F}\right)$$

$$\boxed{\gamma_{conv} \equiv \frac{\sqrt{2q\varepsilon N_a}}{C_{ox}}}$$

We did not use this definition!

- Valid only for uniformly-doped MOSFET
- Hard to estimate ΔV_{th} (Unit is $V^{1/2}$)

Definition of Body Effect Factor



$$\boxed{\gamma \equiv \frac{|\Delta V_{th}|}{|\Delta V_{bs}|}}$$

Then, $\Delta V_{th} = \gamma |\Delta V_{bs}|$

Moreover, $\gamma \approx \dfrac{C_d}{C_{ox}}$

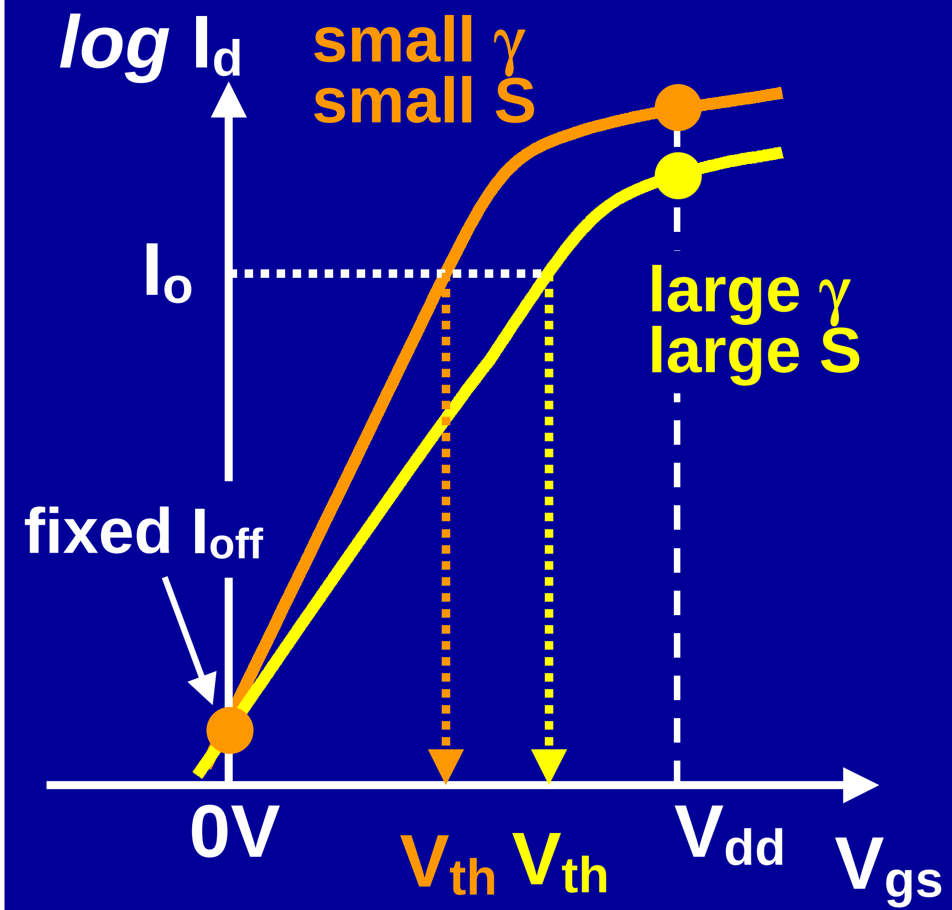
(C_d: depletion cap., C_{ox}: oxide cap.)

Good approximation in
- super steep retrograde profile
- very low ΔV_{bs}

- Directly related to ΔV_{th}
- Applicable to any devices
- Also related to device performance

Relation between Device Performance and γ (1)

Subthreshold characteristic



(for long channel device)

$$\begin{cases} S = 60\left(1+\dfrac{C_d}{C_{ox}}\right) \\ \gamma \approx \dfrac{C_d}{C_{ox}} \end{cases}$$

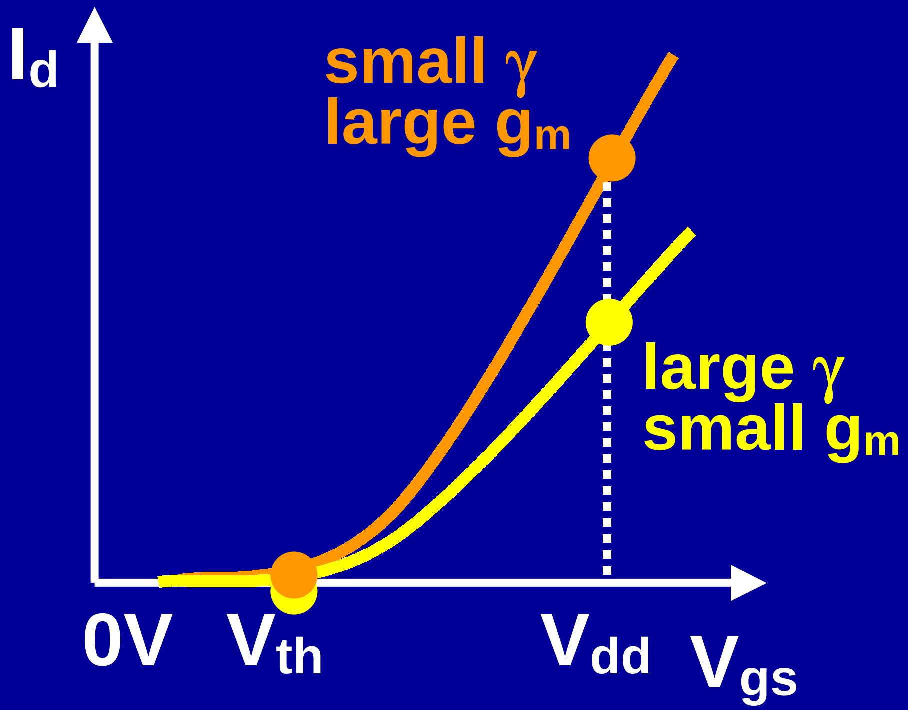
$$\Rightarrow \boxed{S \approx 60(1+\gamma)}$$

	small γ	large γ
S factor	small	large
V_{th} *	low	high

* for fixed I_{off}

Relation between Device Performance and γ (2)

Transconductance



(for long channel device)

$$I_{dsat} = \mu_{eff} C_{ox} \frac{W}{L} \frac{(V_{gs} - V_{th})^2}{2(\underline{1+\gamma})}$$

Charge loss due to the body effect

	small γ	large γ
g_m	large	small
I_{on} *	high	low

* for fixed V_{th}

Trade-off between V_{th} Control and Device Performance

Larger γ device can achieve larger ΔV_{th}

↕ *trade-off*

Larger γ device has lower I_{on} due to
- **larger S factor (→ higher V_{th})**
- **smaller transconductance (g_m)**

↓

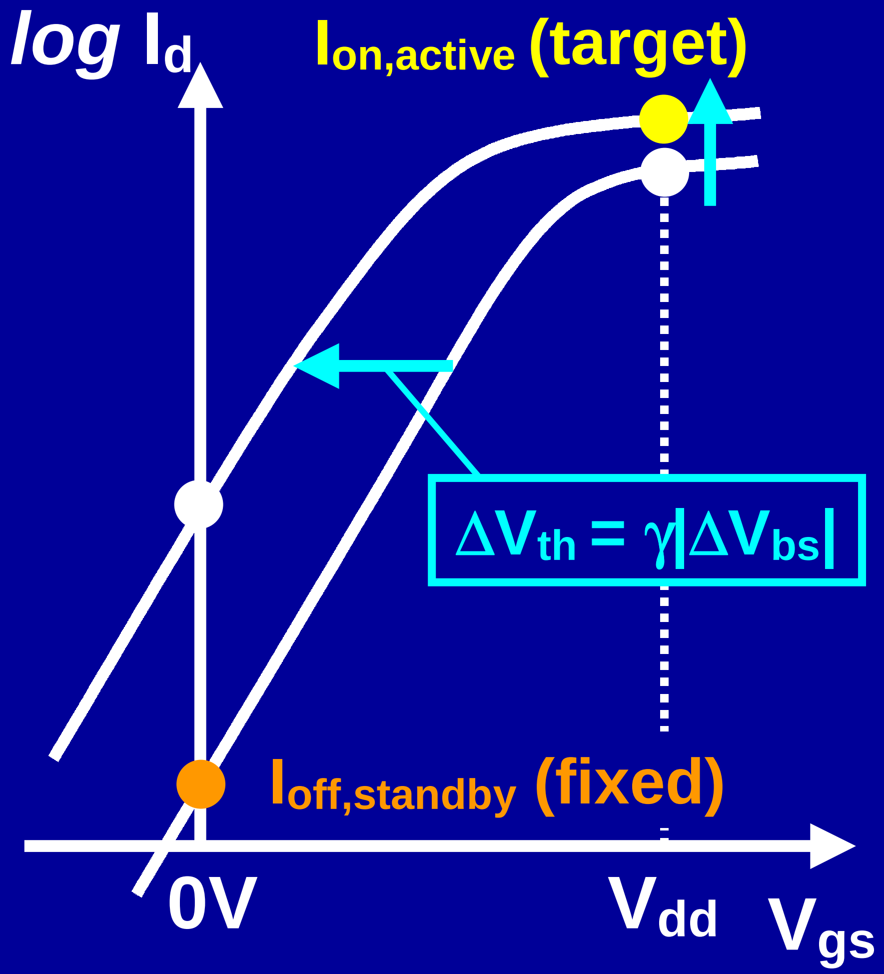
How should we design the device in VTCMOS?

→ **Systematical investigation by means of device simulation**

Outline

- Background and objective
- Body effect factor and its relationship with device characteristics
- Device design in VTCMOS
  - Single devices
  - Series connected circuits
- Effect of velocity saturation
- Summary

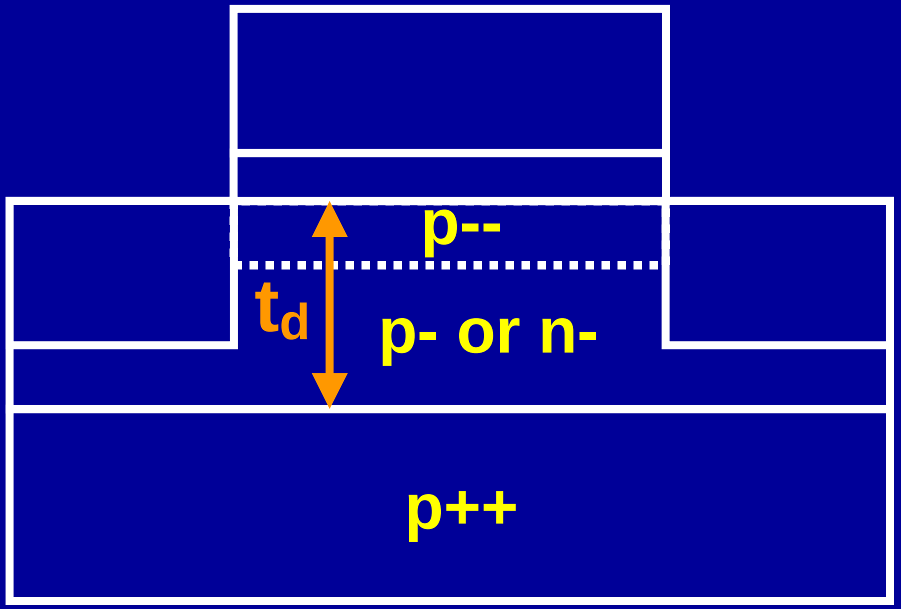
Simulation Procedure

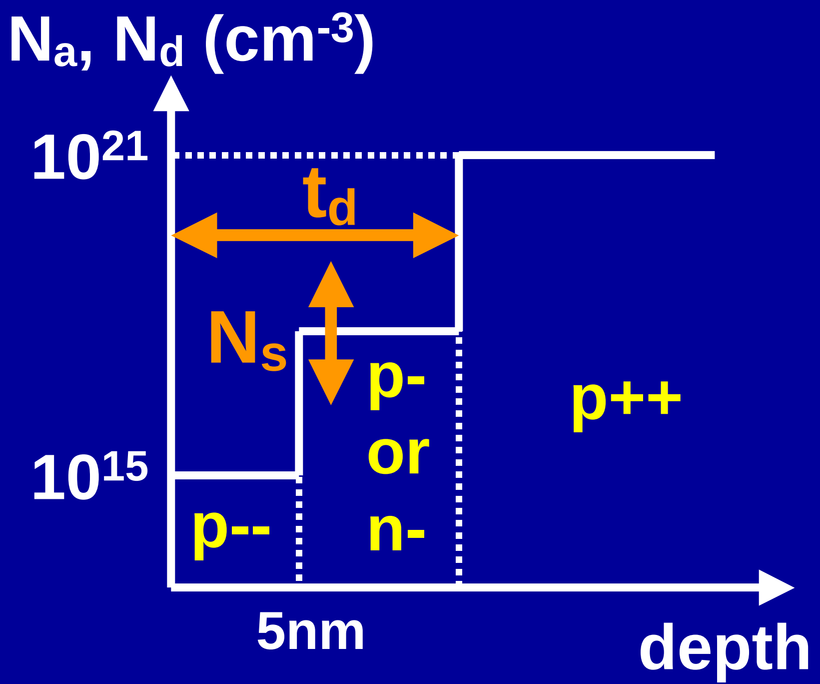


- With fixed $I_{off,standby}$, $I_{on,active}$ is compared.
- γ and $|\Delta V_{bs}|$ are varied separately.

How can we achieve higher on-current?

Device Structure



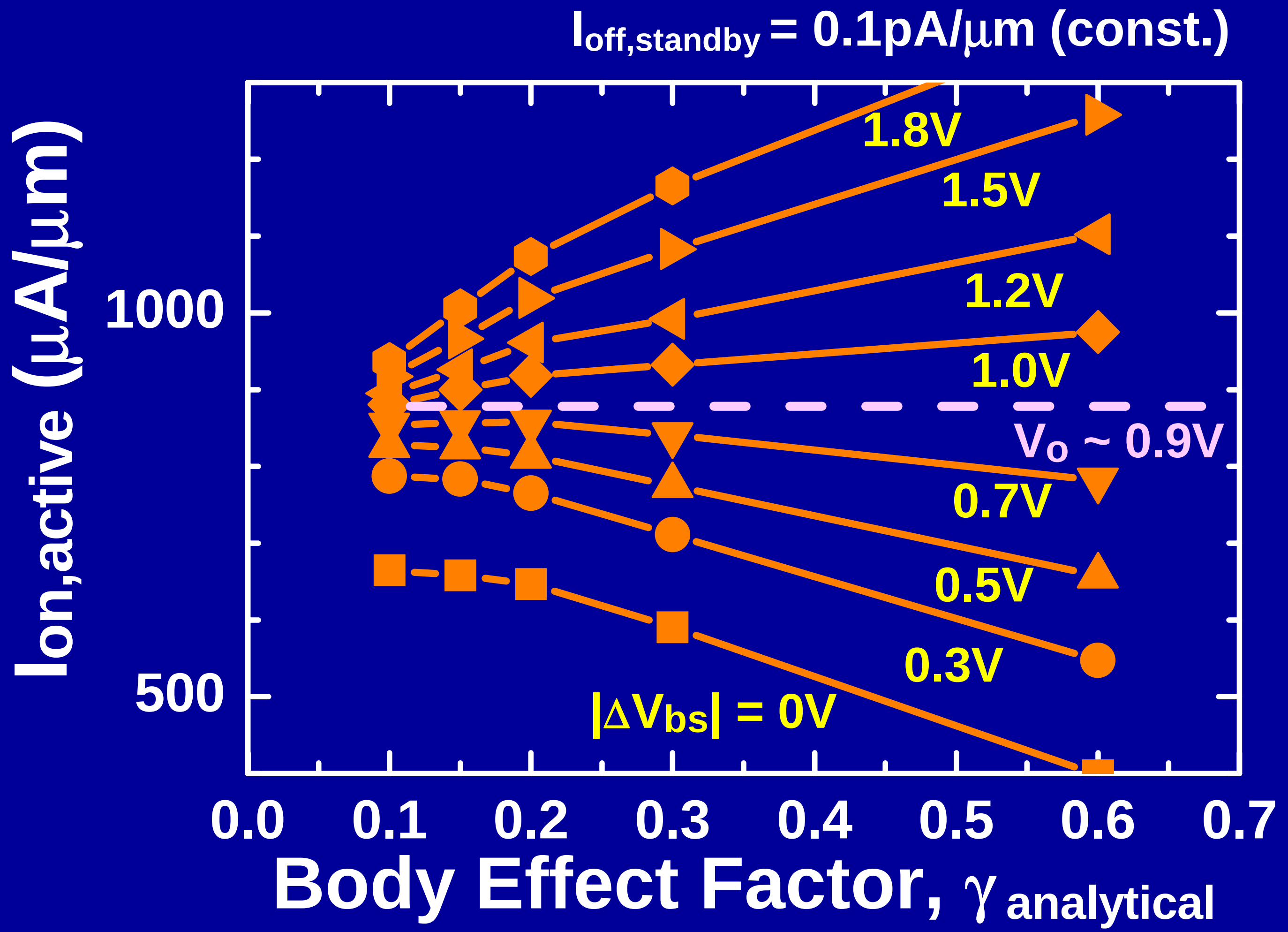


$$\gamma_{analytical} = \frac{C_d}{C_{ox}} \approx 3\frac{t_{ox}}{t_d}$$

Ideal step-shape channel profile

- t_d is varied to change γ.
- N_s is varied to change V_{th} so that $I_{off,standby}$ would be fixed for given $|\Delta V_{bs}|$.
- Non-doped layer (5nm thick) is inserted to avoid inaccuracy of model for impurity dependence of mobility.

γ Dependence of *On*-current

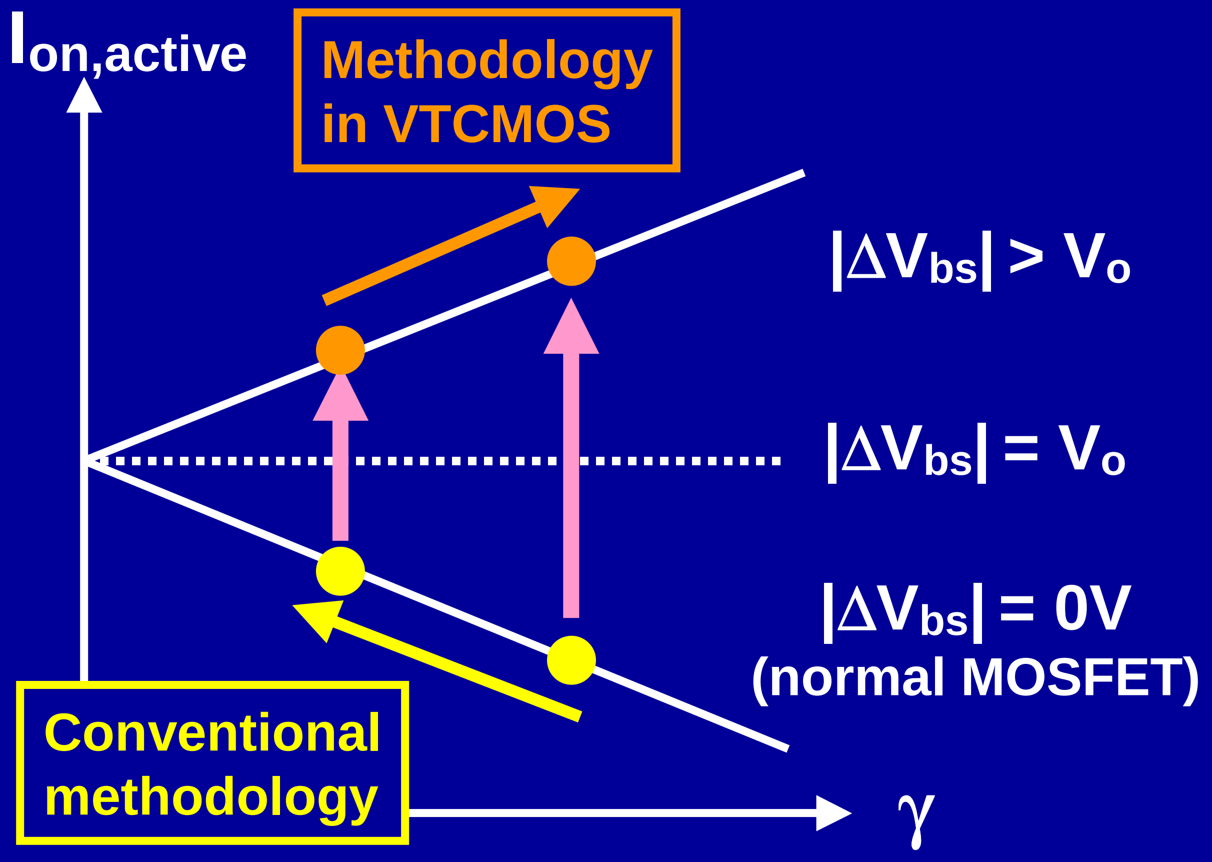


When $|\Delta V_{bs}| < V_o$, larger γ device has lower $I_{on,active}$.

When $|\Delta V_{bs}| > V_o$, larger γ device has higher $I_{on,active}$.

Design Methodology in VTCMOS

- Single Devices -

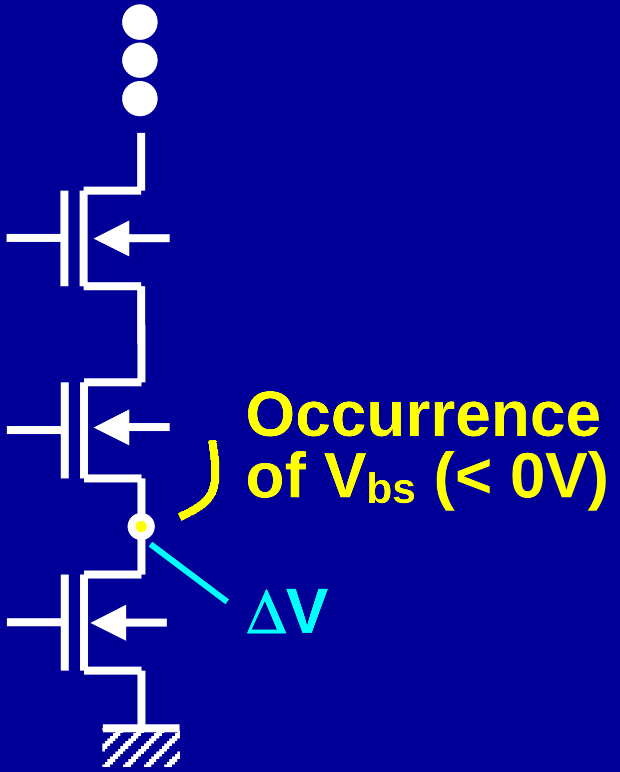


Contradictory to the conventional methodology,
γ should be as large as possible in VTCMOS
when $|\Delta V_{bs}| > V_o$ from the viewpoints of $I_{on,active}$.

Outline

- **Background and objective**
- **Body effect factor and its relationship with device characteristics**
- **Device design in VTCMOS**
  - **Single devices**
  - **Series connected circuits**
- **Effect of velocity saturation**
- **Summary**

Series Connected Circuits



Some source nodes are not connected to GND lines but floating.

↓

Negative substrate bias ($V_{bs} < 0V$) occurs even in **active mode**.

↓

Circuit performance is deteriorated by **the body effect**.

↓

Advantage of large γ device in VTCMOS might be cancelled out in series connected circuits.

→ Further investigation in consideration of the series connected circuits

Evaluation of Performance in Series Connected Circuits

Degradation Factor : F_d

$$F_d \equiv \frac{I_{on}}{I_{on,N}}$$

I_{on} : *on*-current of single device
$I_{on,N}$: *on*-current of series connected circuit

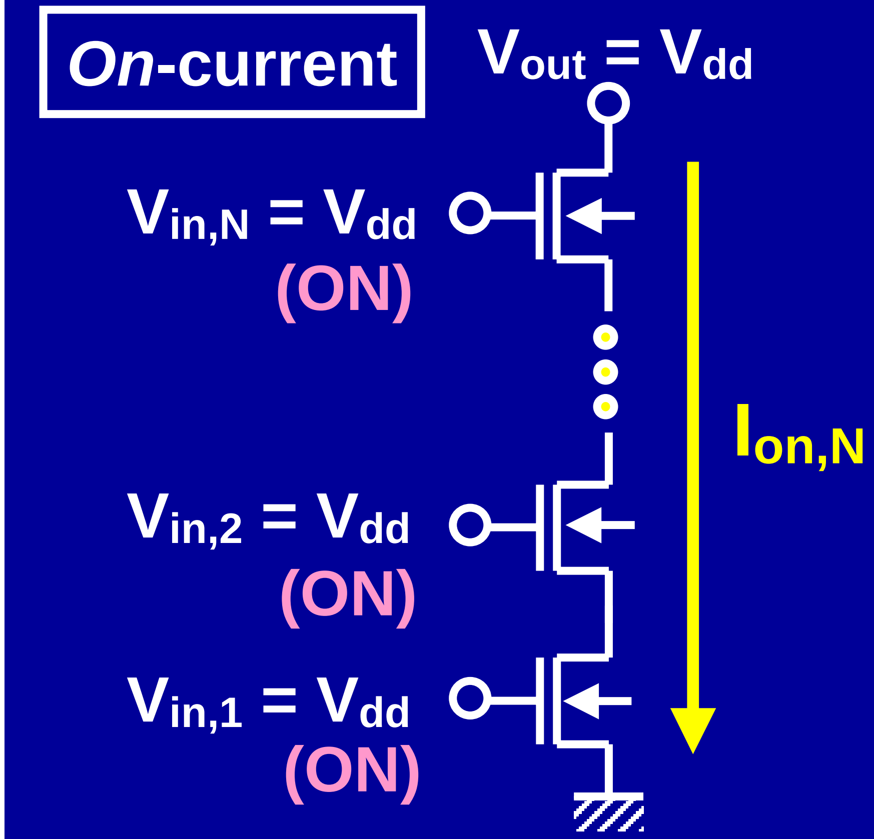
$$= 1 + \frac{1 - 1/\sqrt{2}}{1 - 1/\sqrt[\alpha]{2}} \frac{V_{dsat}}{V_{dd} - V_{th}} (1+\gamma)(1+\lambda V_{dd})(N-1)$$

$$\approx 1 + \frac{1}{2}\alpha \frac{V_{dsat}}{V_{dd} - V_{th}} \underline{(1+\gamma)}(1+\lambda V_{dd})(N-1)$$

Degradation due
to the body effect

[ref.] T. Sakurai *et al*. IEEE JSSC, 26, 122 (1991).

On- and *Off*-currents in Series Connected Circuits



***On*-current**

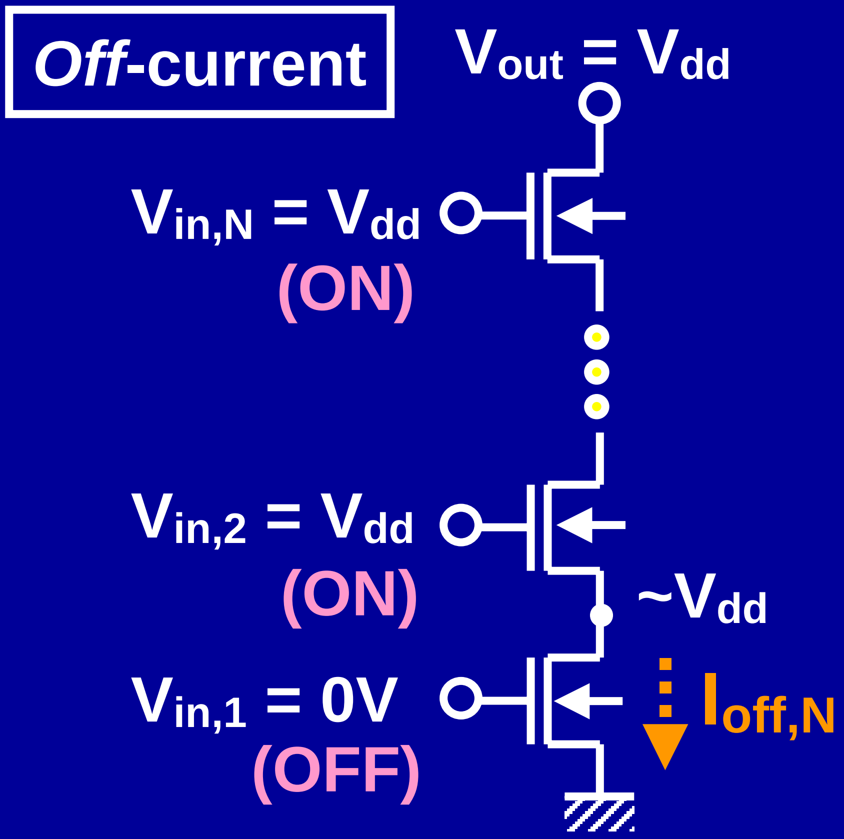
$V_{out} = V_{dd}$

$V_{in,N} = V_{dd}$ (ON)

$V_{in,2} = V_{dd}$ (ON)

$V_{in,1} = V_{dd}$ (ON)

$I_{on,N}$



***Off*-current**

$V_{out} = V_{dd}$

$V_{in,N} = V_{dd}$ (ON)

$V_{in,2} = V_{dd}$ (ON)

$\sim V_{dd}$

$V_{in,1} = 0V$ (OFF)

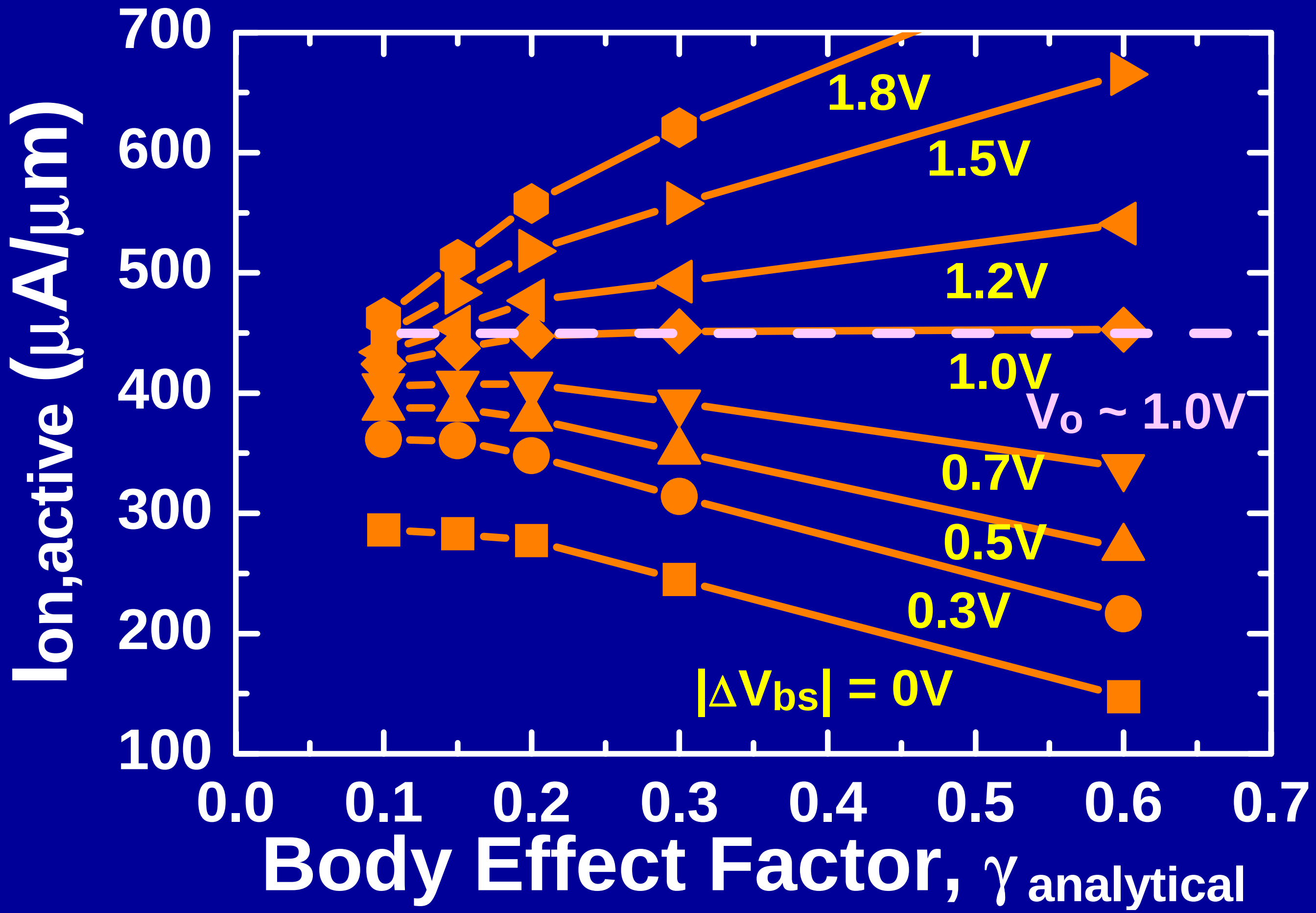
$I_{off,N}$

Worst case *off*-current is almost same as *off*-current of single devices.

➡ Same boundary condition (fixed $I_{off,stanby}$) can be used.

γ Dependence of *On*-current in Series Connected Circuits

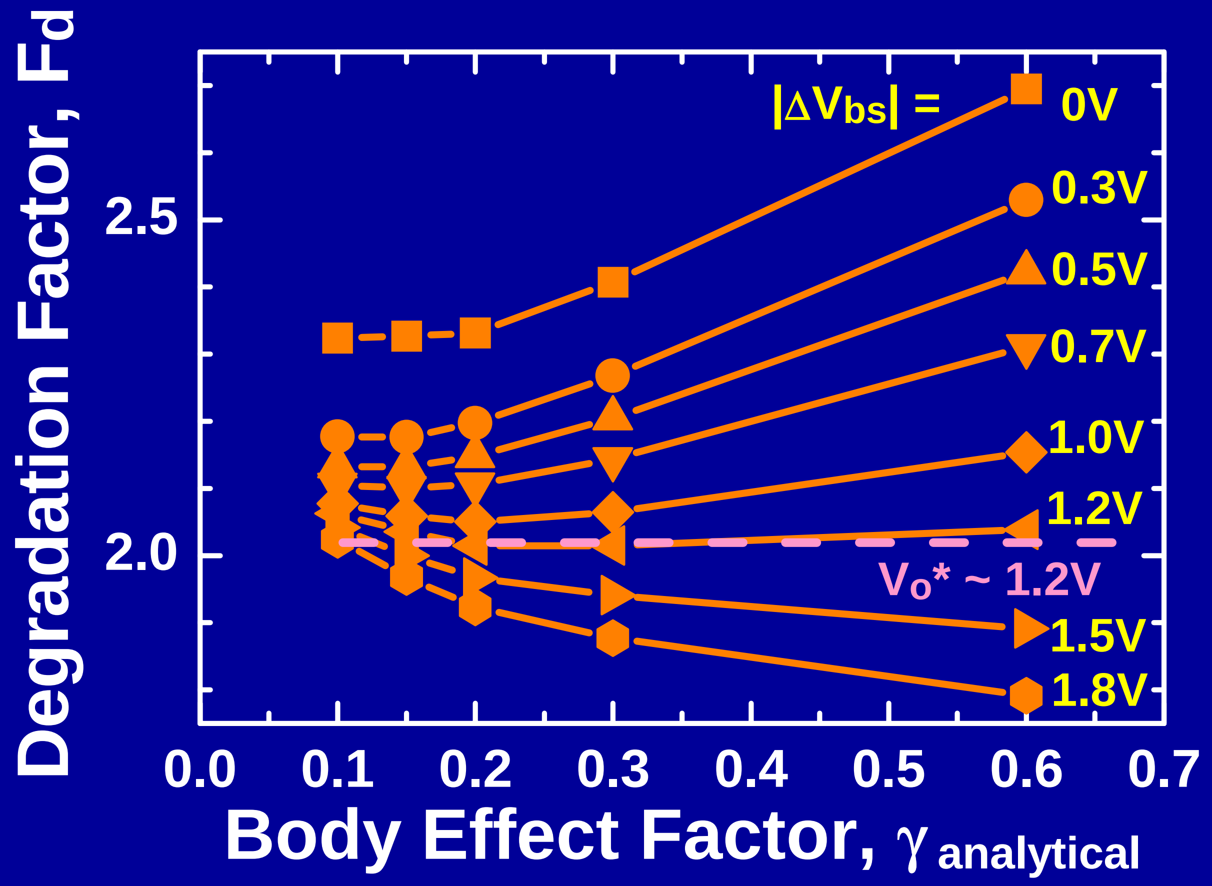
$I_{off,standby}$ = 0.1pA/μm (const.)



\# of Tr. = 3

Although V_o becomes higher (from 0.9V to 1.0V), larger γ device keeps its advantage when $|\Delta V_{bs}| > V_o$.

γ Dependence of F_d



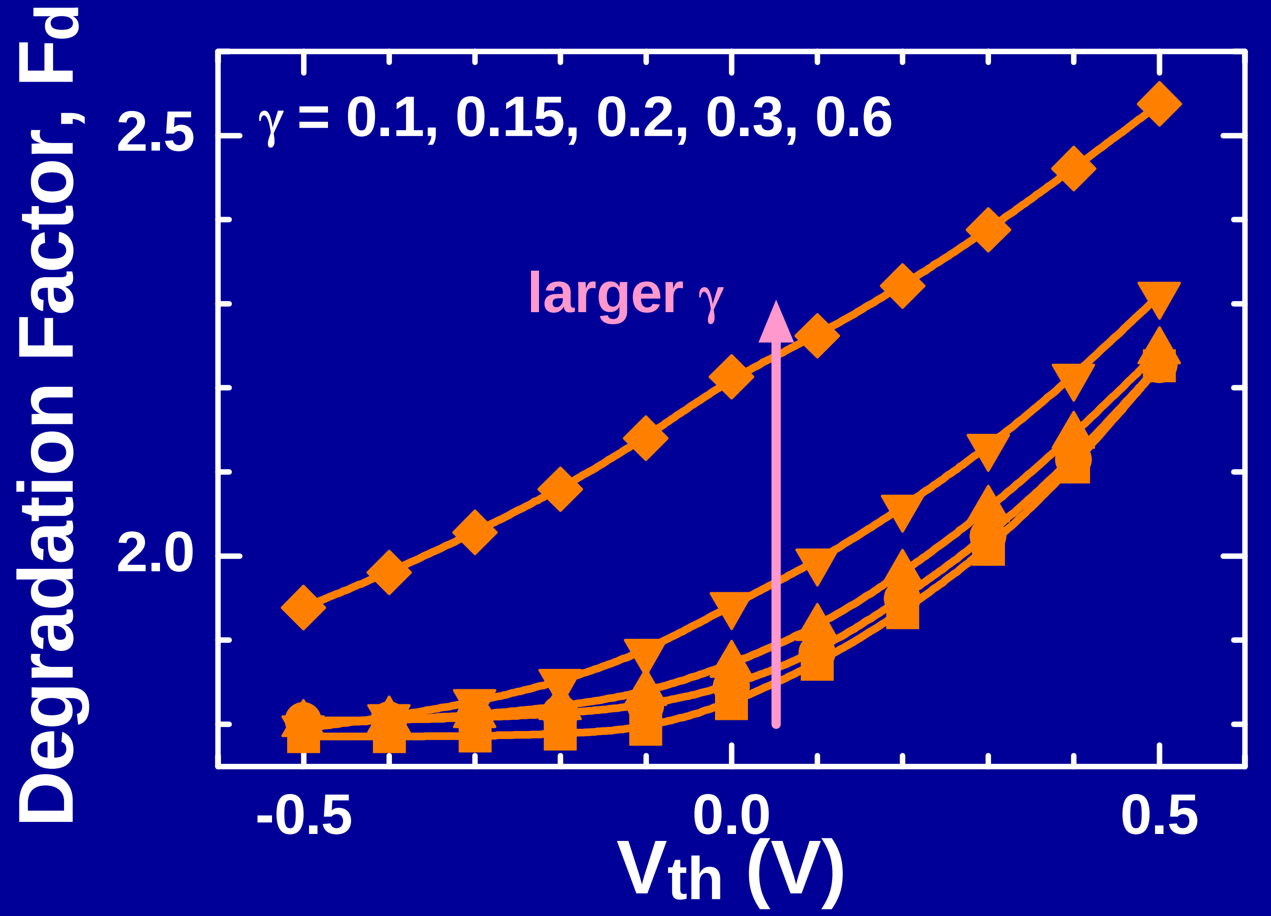
# of Tr. = 3

$$\boxed{F_d \equiv \frac{I_{on}}{I_{on,N}}}$$

- **Utilizing VTCMOS, F_d decreases in each γ value.**
- **As $|\Delta V_{bs}|$ increases above another critical value ($V_o^* \sim 1.2V$), γ dependence of F_d changes.**

→ ***Larger γ device has smaller F_d !?***

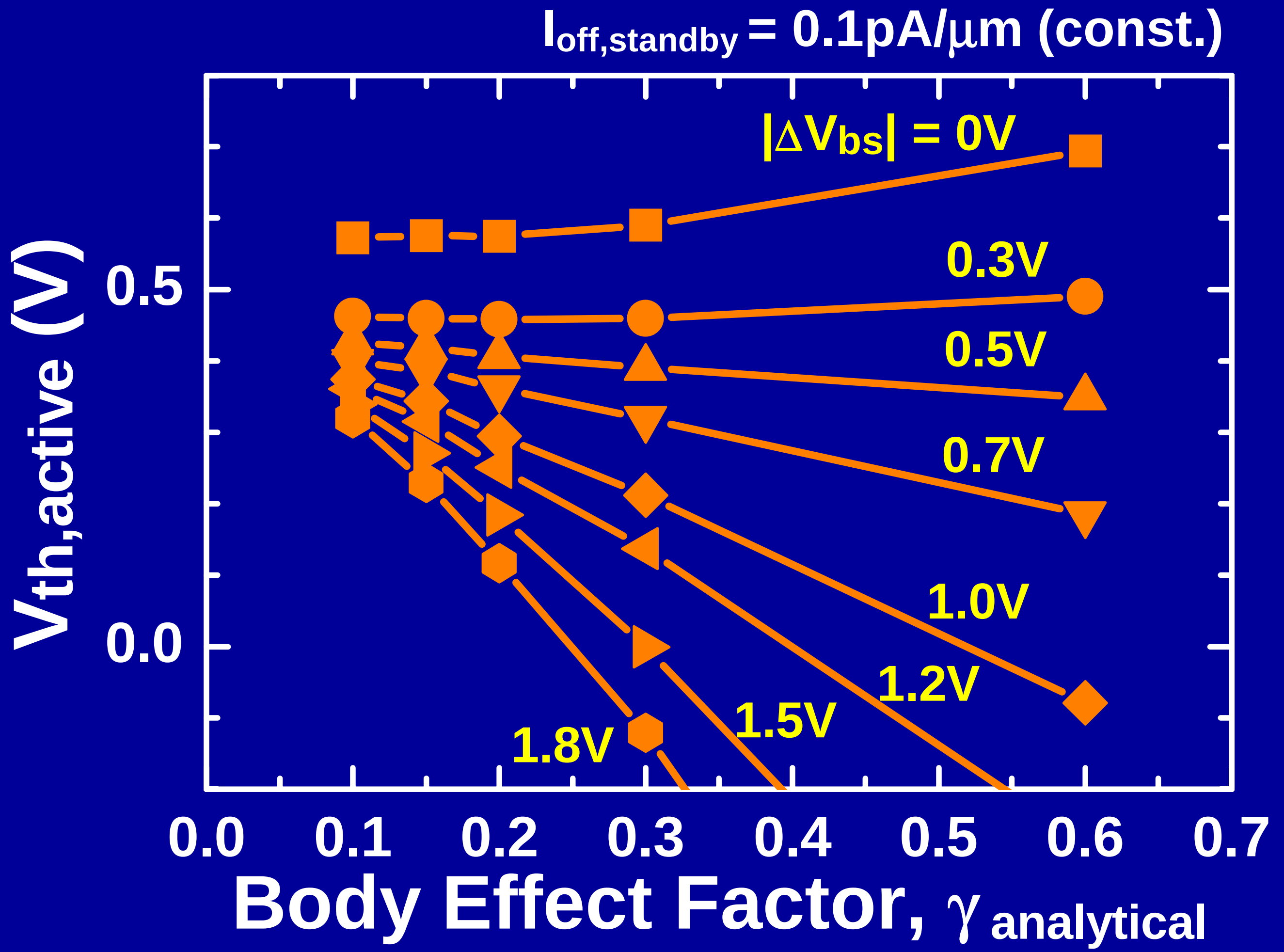
Effect of Lowering V_{th}



- With the constant V_{th}, larger γ has larger F_d.
- In any γ values, lowering V_{th} results in decrease of F_d.

γ Dependence of Active V_{th}

$I_{off,standby}$ = 0.1pA/μm (const.)



Larger γ device can achieve lower V_{th} in active mode with the fixed stand-by *off*-current.

→ ***Smaller F_d in spite of larger body effect***

Design Methodology in VTCMOS

- Series Connected Circuits -

On-current in the series connected circuits

$$\boxed{I_{on,N} = \frac{I_{on}}{F_d}}$$

VTCMOS can not only enhance I_{on} but also reduce F_d by lowering V_{th}.

→ Larger enhancement of I_{on} in the series connected circuits

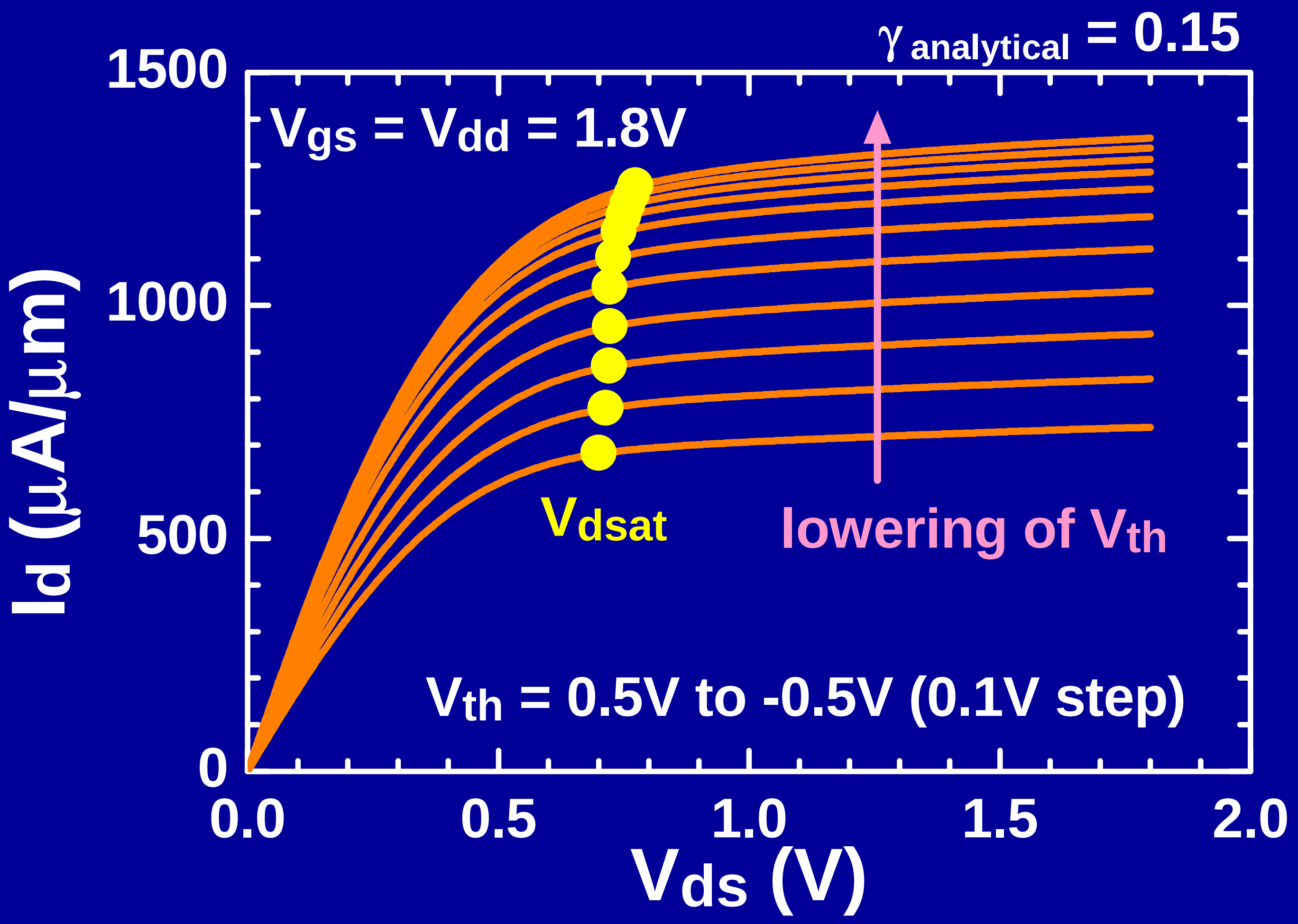
Larger γ device can achieve lower $V_{th,active}$, resulting in smaller F_d.

→ Advantage of large γ device in VTCMOS is not cancelled out but rather enhanced in the series connected circuits.

Outline

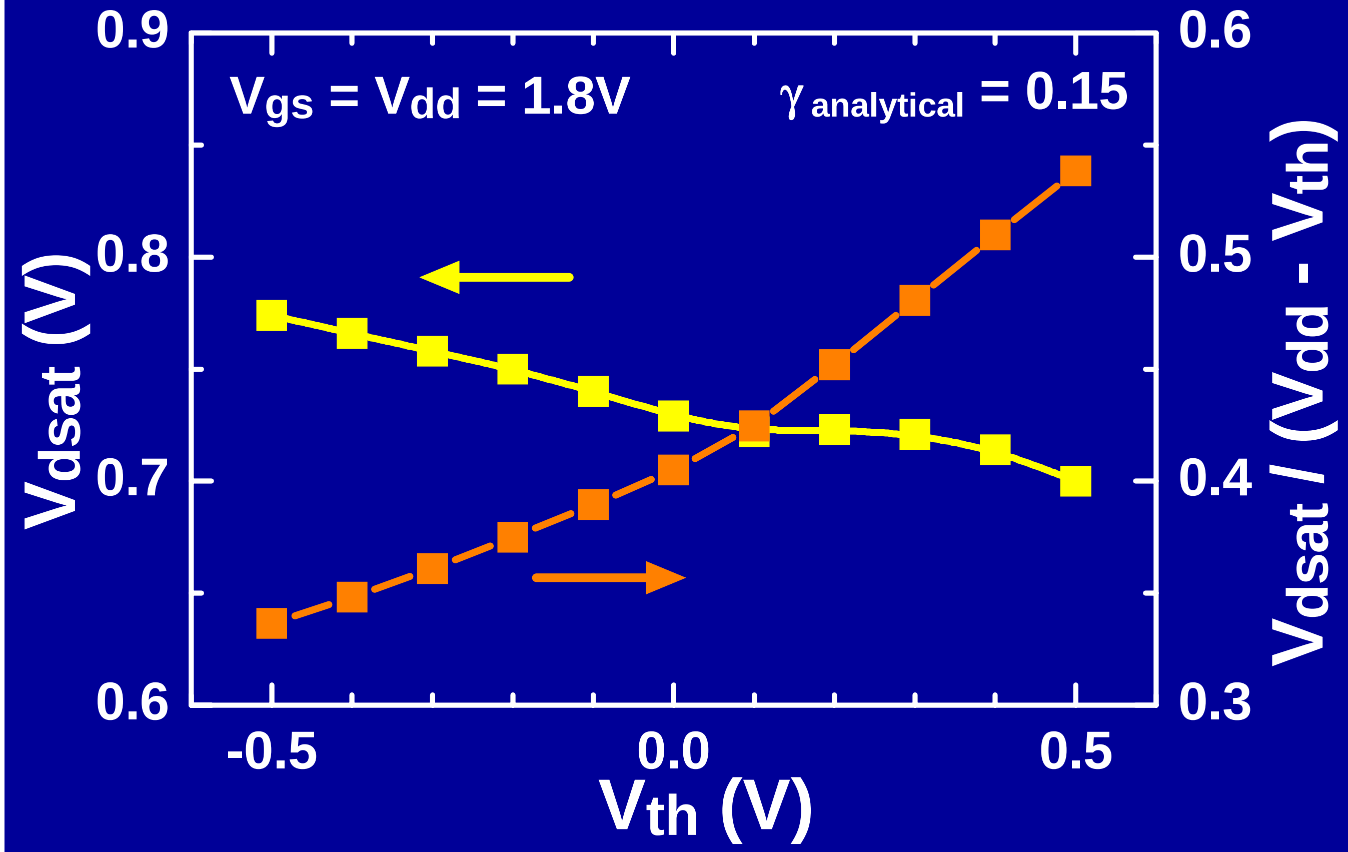
- Background and objective
- Body effect factor and its relationship with device characteristics
- Device design in VTCMOS
  - Single devices
  - Series connected circuits
- **Effect of velocity saturation**
- Summary

Effect of Velocity Saturation



As V_{th} decreases, V_{dsat} only slightly increases due to velocity saturation phenomenon.

Mechanism of F_d Reduction



$$F_d \approx 1+\frac{1}{2}\alpha\boxed{\frac{V_{dsat}}{V_{dd}-V_{th}}}(1+\gamma)(1+\lambda V_{dd})(N-1)$$

Slight increase of V_{dsat} with lowering V_{th}

V_{dsat} / (V_{dd} - V_{th}) decreases

F_d decreases !!

Summary

- VTCMOS characteristic is systematically investigated by means of device simulation.

- From the viewpoint of device performance, larger γ device can achieve higher *on*-current, when $|\Delta V_{bs}|$ is larger than a certain critical value.

- Lowering V_{th} alleviates the degradation due to the series connected configuration. Therefore, when $|\Delta V_{bs}|$ is applied to some extent, larger γ device has higher *on*-current even in the series connected circuits.

- These characteristics are attributed to the velocity saturation phenomenon which makes the drain saturation voltage less sensitive to V_{th}.