VTCMOS characteristics and its optimum conditions predicted by a compact analytical model

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ABSTRACT

A very compact analytical model of variable threshold voltage CMOS (VTCMOS) is proposed to study the *active on-current*, linking it with the *stand-by off-current* characteristics. Comparisons of modeled results to numerical simulations and experimental data are made with an excellent agreement. It is clearly demonstrated using the model that speed degradation due to low supply voltage can be compensated by the VTCMOS scheme with even smaller power. Influence of the short channel effect (SCE) on the performance of VTCMOS is investigated in terms of a new parameter, $dS/d\gamma$, both qualitatively and quantitatively. It is found that the SCE degrades the VTCMOS performance. Issues on the optimum conditions of VTCMOS are discussed.

Keywords

Body Effect, Variable threshold voltage CMOS (VTCMOS), Substrate bias, Low power, and Analytical model

1. INTRODUCTION

Very recently, a new functional CMOS device called Variable Threshold Voltage MOSFET (VTCMOS) has promised to be amongst the next generation of ultra-low power devices operating at low supply voltage [1-3]. The operating principle of VTCMOS is that its threshold voltage (V_{th}) is controlled by the applied substrate bias ($-|V_{bs}|$), leading to lower stand-by off current or higher active on-current. The V_{th} shift is given by: $\Delta V_{th} = \gamma |V_{bs}|$ where γ is the body effect factor [4]. The optimal function of the device is to significantly reduce the stand-by *off*-current keeping high active *on*-current, or to enhance the active *on*-current keeping low stand-by current, both of which are indispensable for obtaining high-speed low-power performance. However, it is very difficult to design a VTCMOS satisfying these most requirements, in particular in case of short channel devices whose threshold voltage and effective channel length are hardly predictable. As CMOS technology advances leading to more and more delicate VTCMOS structure, it becomes tedious and complicated to analytically predict VTCMOS' characteristics.

Recently, although Koura *et al* reported simulation results of the performance of VTCMOS to find optimum conditions [5], physical interpretation of the optimum parameters, characteristic features and scalability of VTCMOS are still unclear. To our best knowledge, no analytical VTCMOS model has been reported to investigate both of the currents simultaneously.

In this study, we introduce an analytical formula to predict the active and stand-by *off-currents* characteristics of VTCMOS. The formula is very compact and valid in a wide range of channel lengths. In order to explore the relation between the *active on*-current ($I_{on}(a)$) and *active off*-current ($I_{off}(a)$) at a desired *stand-by off*-current ($I_{off}(s)$), we adapt the α-power law model [6] that is widely used by circuit designers. Since these two models are very compact and easy to use, they will be well integrated and practical for low-power circuit designers. The VTCMOS model is compared by numerical simulations and successfully verified by experimental data collected from devices with channel lengths between 4μm and 0.1μm. For the first time, the VTCMOS gate delay time and active power are systematically studied and the influence of the short channel effect (SCE) is discussed.

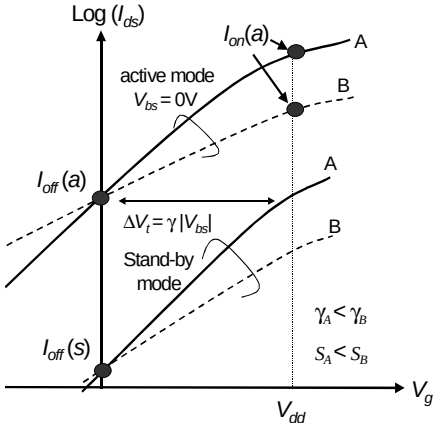

Figure 1. Schematic description of the characteristics of VTCMOSs whose γ and *S* are different. For easy comparison and simplicity, off-currents in the stand-by and active modes are set the same. Device A has higher on-current ($I_{on}(a)$) due to its smaller *S* but requires larger V_{bs} than device B to attain the same stand-by off current ($I_{off}(s)$) due to the smaller γ. This is quantitatively understood using (2) and (3) in the text.

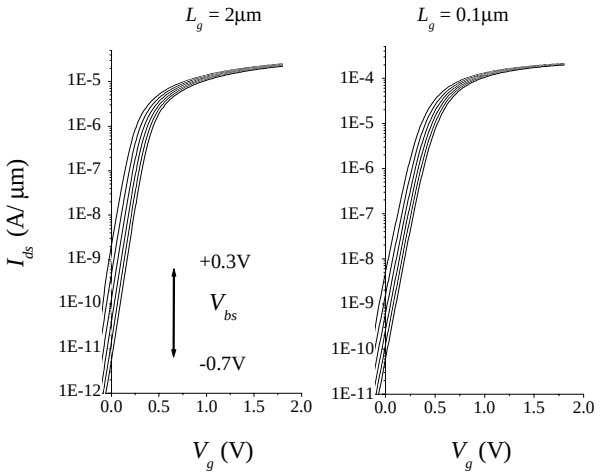

Figure 2. Measured I_{ds} *versus* V_g characteristics of *n*-type MOSFETs as a function of V_{bs}. 10mV V_{ds} was applied for the measurements.

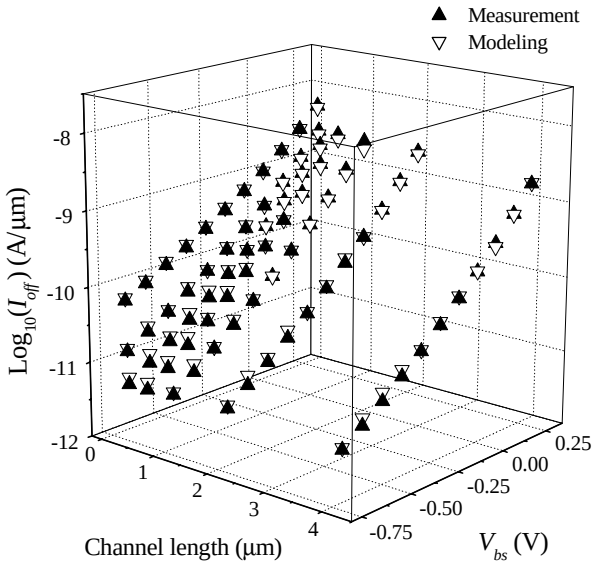

Figure 3. Comparison between the measured and modeled I_{off} (*s*) data as a function of V_{bs}. Note that the modeled results are also in excellent agreement in the positive substrate bias (+V_{bs}) regime.

2. VTCMOS MODEL AND EVALUATION

Fig 1 shows schematic I_{ds}–V_g characteristics of different VTCMOSs. The performance of a VTCMOS is mainly determined by γ and subthreshold slope (*S*) defined by $(d\log_{10}I_{ds}/dV_g)^{-1}$ at a given $|V_{bs}|$. When γ is larger, ΔV_{th} becomes larger, and the *off*-current can be more suppressed or the *on*-current can be more enhanced. On the other hand, when *S* is degraded, V_{th} should be larger to suppress the *off*-current and *on*-current is reduced.

In this study, γ is defined as $|\Delta V_{th}/V_{bs}|$. To avoid confusion, the substrate sensitivity is denoted as Γ (namely, dV_{th}/dV_{bs} at V_{bs} = 0V), which can be given by the ratio of the gate oxide and depletion layer capacitances ($\Gamma=C_D/C_{ox}$). γ is smaller than Γ. For a long channel MOSFET at room temperature, *S* can be expressed in terms of Γ and γ:

$$\begin{aligned} S &= 60\,(1+\Gamma) \\ &= S_0\,(1+\gamma) \end{aligned} \qquad \text{(in the unit of mV/decade)} \quad (1)$$

where S_0 ($=dS/d\gamma$) is larger than 60. This equation indicates that a device with a larger γ has a larger *S*. However, when the SCE takes place, γ becomes smaller but *S* increases, consequently resulting in the failure of the above $S-\gamma$ relation and $dS/d\gamma$ decreases. New empirical relation between them is proposed in this paper and will be detailed in the relevant section.

The main purpose of the VTCMOS model is to find the relations among $I_{on}(a)$, $I_{off}(a)$ and $I_{off}(s)$ as a function of γ, *S* and V_{bs}, and subsequently to propose the best performance conditions of a VTCMOS. In this paper, the stand-by *off*-current is fixed and the active *on*-current is evaluated to attain the high speed characteristics.

Off-current model

In the subthreshold regime, the *off*-current is characterized by the diffusion transport. Using the definition of *S*-factor ($\approx (\Delta\log_{10}I_{ds}/\Delta V_g)^{-1}$) and *off*-currents, the threshold voltages defined as gate voltages when current reaches $10^{-\Omega}$ *W/L* can be expressed:

$$V_{th} = S\log_{10}\left(\frac{10^{-\Omega}}{I_{off}(a)}\frac{W}{L}\right) \text{ and } V_{th}^{/} = S^{/}\log_{10}\left(\frac{10^{-\Omega}}{I_{off}(s)}\frac{W}{L}\right), \quad (2)$$

where Ω is an empirical parameter that depends on the definition of V_{th} and is in general around 7. $V_{th}^{/}$ and $S^{/}$ are the corresponding parameters in the stand-by mode. Note that $V_{th}^{/} = V_{th} + \gamma|V_{bs}|$. By rearranging the equations, the ratio of the *off*-currents in the active and stand-by modes is given by:

$$r \equiv \frac{I_{off}(a)}{I_{off}(s)} = 10^{\frac{V_{th}^{/}}{S^{/}} - \frac{V_{th}}{S}} = 10^{\frac{\eta\gamma|V_{bs}|}{S}}, \quad (3)$$

where $\eta > 1$, but $\eta \approx 1$ unless *S* is significantly improved under an applied substrate bias. The ratio, *r*, is a key factor to understand VTCMOS and is very practical to use since structural parameters such as channel length, width and oxide thickness are not included in the ratio equation.

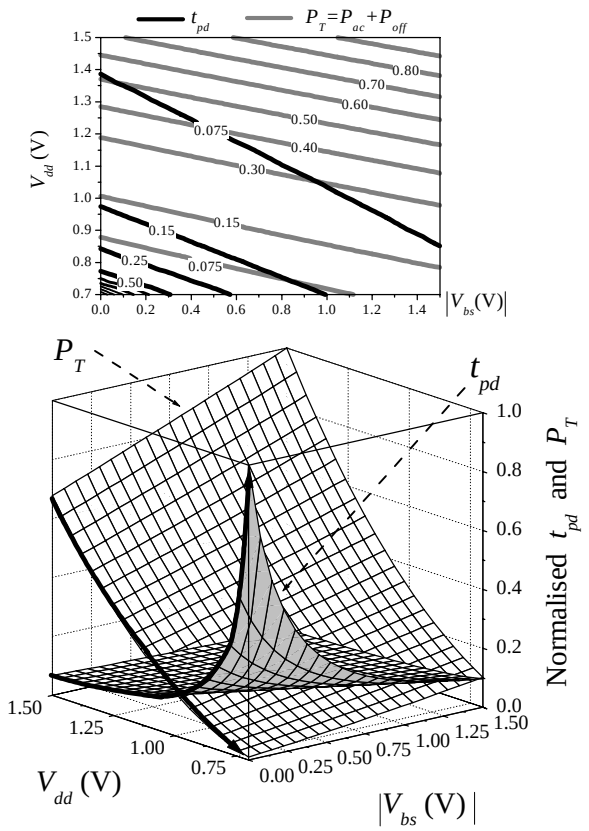

Figure 4. Normalized gate delay time (t_{pd}) and total power (P_T) as a function of V_{bs} and V_{dd} at a constant I_{off}(s) of 10^{-13} A/μm. In these calculations, S = 80mV/decade, γ = 0.2 and α =1.3 are used. The upper plot shows the contour lines of t_{pd} and P_T in the V_{bs} – V_{dd} plane

To verify the validity of the ratio equation, the current-voltage characteristics of MOSFETs with channel lengths ranging from 4μm to 0.1μm were measured. Two examples of the measurements are shown in Fig 2. As seen in Fig 3, the measured I_{off}(s) data are in excellent agreement with the modeled I_{off}(s) calculated using (3), in a wide range of channel lengths.

2.1 On-current model

The α-power law model proposed by Sakurai *et al* is the most widely used drain current model due to its compact mathematical form and high degree of accuracy [6]. In this paper, incorporating the α-power model the *active on* current of VTCMOS is given by:

$$I_{on}(a) = B \cdot (V_{dd} - V_{TH})^{\alpha}. \quad (4)$$

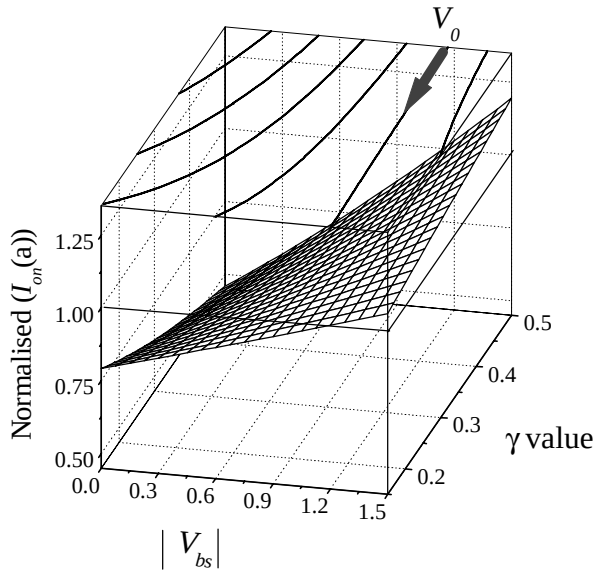

Figure 5. Calculated $I_{on}(a)/I_o$ and its contour map onto the γ–V_{bs} plane. In this calculation, the values of α and V_{dd} are 1.5 and 1.5V respectively. I_{off}(s) is fixed at a 10^{-13} A/μm.

For the long channel case, B should be close to the value of $\mu_{eff} C_{ox} \cdot W/L/2(1+\Gamma)$ and α to 2. If the SCE is not severe, B is expected to be proportional to 1/(1+γ). The effect of γ on α is relatively negligible compared with those of V_{TH} and B. The threshold voltage, V_{TH}, is not necessarily the same with conventionally used ones. Instead, the following relation is fulfilled:

$$V_{TH} = V_{th} + \Theta, \quad (5)$$

where Θ is a constant [7]. From (2), when I_{off}(s) = 10^{-13} A/μm, V_{TH} is given by:

$$\begin{aligned} V_{TH} &= S \cdot \log_{10}\left(\frac{10^{-\Omega}}{10^{-13} \cdot r} \cdot \frac{W}{L}\right) + \Theta \\ &= [S(13 - \Omega') - \eta\gamma |V_{bs}|], \end{aligned} \quad (6)$$

where Ω' is also a constant regardless of the definition method of V_{th}. Resultantly, $I_{on}(a)$ becomes a function of targeted I_{off}(s) and other key parameters.

3. VTCMOS CHARACTERISTICS

Concerning the speed performance of VTCMOS circuits, the gate delay time is the most crucial factor. In CMOS digital circuits, the gate delay time (t_{pd}) is given by:

$$t_{pd} \propto \frac{C_L V_{dd}}{I_{on}(a)} \cong \frac{A \cdot C_L \cdot V_{dd}}{(V_{dd} - V_{TH})^{\alpha}}, \quad (7)$$

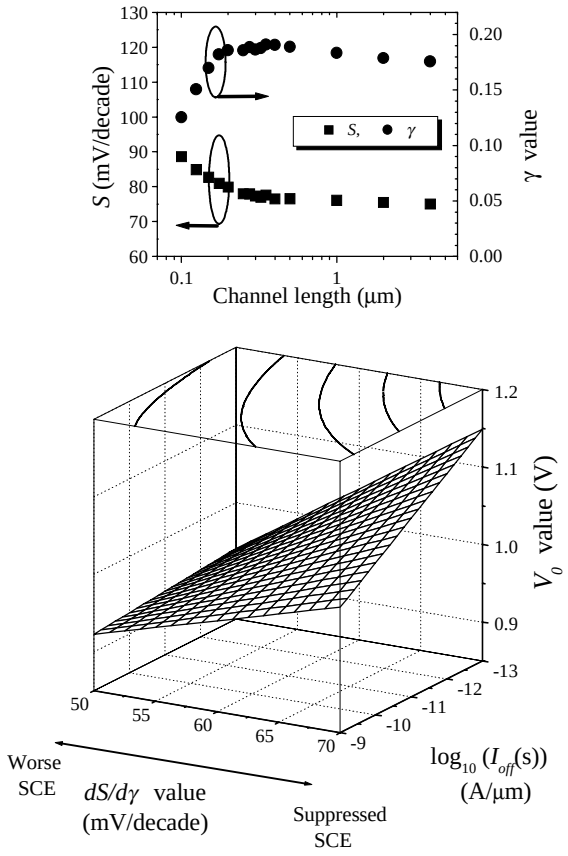

Figure 6. Calculation of the characteristic $|V_{bs}|$ ($=V_0$). $\gamma = 0.3$ and $V_{dd} = 1.5$V. The upper plot shows the measurements of *S*, and γ values as a function of channel length. Equation (10) is used for $dS/d\gamma$.

where C_L is the load capacitance, and A is a constant. Fig 4 shows the calculation of the normalized gate delay time of VTCMOS, together with that of the total power in the active mode ($P_T = P_{ac} + P_{off}$) under the same conditions. The stand-by *off*-current is fixed (10^{-13} A/μm). The thick lines at $V_{bs} = 0$ indicate the normalized t_{pd} and P_T characteristics of a normal CMOS as a function of V_{dd}. As V_{dd} decreases, t_{pd} increases rapidly. However, by applying V_{bs}, t_{pd} is rapidly recovered. Larger V_{bs} denotes a lower threshold voltage, leading to higher $I_{on}(a)$ current and therefore to smaller gate delay time.

The upper inset of Fig 4 shows the contour lines of normalized t_{pd} and P_T. It is clearly shown from this contour plot that the speed degradation at a low V_{dd} can be compensated by applying V_{bs}. Note that as V_{bs} increases P_T decreases even when t_{pd} is constant, indicating that VTCMOS always consumes smaller power than a normal CMOS ($V_{bs} = 0$) at the same speed. This figure clearly demonstrates that the high speed operation with both extremely low active and stand-by powers, which cannot be attained in a normal MOSFET with V_{bs}=0, is fulfilled in the VTCMOS scheme.

Fig 5 shows the modeled $I_{on}(a)$ and its contour map projected onto the $\gamma - V_{bs}$ plane, at a fixed $I_{off}(s)$ of 10^{-13} A/μm. When $|V_{bs}| = 0$ (a normal MOSFET), as γ increases V_{th} increases due to increased S and thus $I_{on}(a)$ decreases. However, when V_{bs} is sufficiently large (for example, $|V_{bs}| = 1.2$V), as γ increases V_{th} decreases, which is predicted from (6), and $I_{on}(a)$ increases. Therefore, there are two completing factors that degrade and enhance $I_{on}(a)$. When the two factors are balanced at a certain $|V_{bs}|$, $I_{on}(a)$ looks rarely-dependent on γ, as shown in Fig 5. We denote the characteristic value of $|V_{bs}|$ as $|V_0|$. $|V_0|$ is very important because its value would give a rough idea for the optimum conditions of the VTCMOS performance. Importantly, when $|V_{bs}|>|V_0|$, as γ increases $I_{on}(a)$ increases, whilst when $|V_{bs}|<|V_0|$ as γ increases $I_{on}(a)$ decreases. Therefore, the optimum value of γ depends on whether the applied substrate bias is larger than $|V_0|$ or not. At a smaller γ value, $I_{on}(a)$ smoothly increases with $|V_{bs}|$. At the extreme case of $\gamma = 0$, $I_{on}(a)$ is given as a constant, I_o which is the same with $I_{on}(a)$ when $|V_{bs}|=|V_0|$. Recent numerical simulations are consistent with these modeling results [5].

The physical origin of $|V_0|$ can be understood by finding a contour line of $I_{on}(a)$ with respect to γ, thus by differentiating (4) with respect to γ:

$$\frac{dI_{on}(a)}{d\gamma} = \frac{dB}{d\gamma}(V_{dd} - V_{TH})^{\alpha} - \alpha B(V_{dd} - V_{TH})^{\alpha-1}\frac{dV_{TH}}{d\gamma}. \quad (8)$$

Rearranging (8), $|V_0|$ is given as $|V_{bs}|$ when $dI_{on}(a)/d\gamma = 0$ at each γ value:

$$|V_0| = \frac{V_{dd} + (\log_{10}(I_{off}(s)^{-1}) - \Omega')[(1+\gamma)\cdot\alpha\cdot dS/d\gamma - S]}{(1+\gamma)\cdot\alpha - \gamma}. \quad (9)$$

As seen in (9), $|V_0|$ is an explicit function of V_{dd}, $I_{off}(s)$, γ, α and S. Most crucial factor in determining $|V_0|$ is the value of V_{dd}, compared with the other parameters. In addition, since the effect of γ on $|V_0|$ is small, $|V_0|$ seems to be a single value independent of γ. For example, with $V_{dd} = 1.5$V, $I_{off}(s)=10^{-13}$A/μm, and α=1.5, variation of γ from 0.2 to 0.5 corresponds to $|V_0| = \sim 1.17$ and ~1.11V, respectively. Most interesting and important note of the analytical expression of $|V_0|$ in (9) is the possible scalability of $|V_0|$ with decreasing V_{dd}. Recent our simulation results are in excellent agreement with this $|V_0|$ dependence on V_{dd}. Full analysis of this study will be reported separately with the simulation results [8].

Fig 6 shows the calculated $|V_o|$ using (9) as a function of targeted $I_{off}(s)$ and $dS/d\gamma$. As $I_{off}(s)$ increases, V_0 decreases as shown. This is because V_{th} in the stand-by mode decreases. Consequently, $I_{on}(a)$ enhancement term (second term in (6)) will be dominant. This means that larger $I_{on}(a)$ enhancement can be obtained in a smaller $|V_{bs}|$. However, $dS/d\gamma$ increases, V_0 increases, as shown in Fig 6. We have found that the value of $dS/d\gamma$ is related to the SCE. We have also found that only in terms of the SCE, $|V_o|$ should be increased. Detailed implication for $dS/d\gamma$ will be further discussed below.

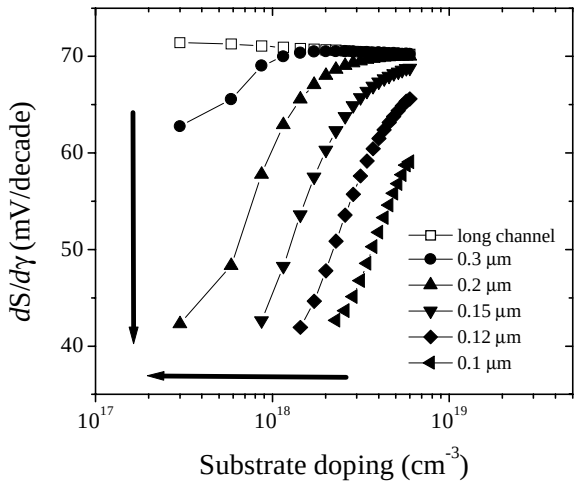

Figure 7. Analytical calculation of $dS/d\gamma$ in an uniformly doped VTCMOS, as a function of channel length and substrate doping concentration. The thick arrows indicate directions where the short channel effect becomes worse. $|V_{bs}| = 1V$. $t_{ox} = 40Å$.

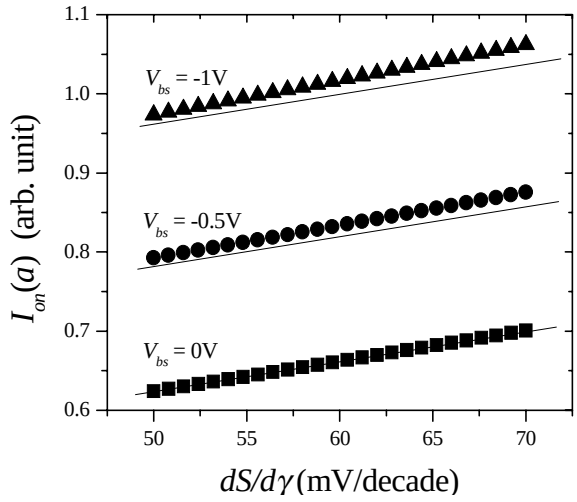

Figure 8. Enhancement of $I_{on}(a)$ at $\gamma = 0.3$ under three different substrate biases, as a function of $dS/d\gamma$. Note that $I_{off}(s)$ is fixed at 10^{-13}A/μm. Other modeling parameters are the same with those used for Fig 5. The three lines represent the slope of $I_{on}(a)$ at $V_{bs} = 0V$.

4. Influence of Short Channel Effect

Once the SCE starts to appear, γ and S are quickly degraded, resultantly leading to a smaller reduction of the stand-by *off* current at a given V_{bs} and to a significantly reduced enhancement of the active *on* current at a targeted stand-by *off* current, as understood from (3), (4) and (6). To simply quantify the SCE on the performance of VTCMOS seems difficult and inefficient. Nevertheless, it would be instructive to anticipate how much the VTCMOS performance would be degraded by the SCE even in a qualitative level, providing some useful guidelines in designing a VTCMOS of high performance. Since γ and S are main parameters of a VTCMOS, it would be the most important to investigate the SCE on them.

Fig 7 illustrates the numerically calculated values of $dS/d\gamma\big|_{N_a}$ (namely, $\left|(dS/dN_a)/(d\gamma/dN_a)\right|$) in an uniformly-doped *n*-type VTCMOS at $|V_{bs}| = 1V$. The SCE is taken into account in the calculations [9]. For all channel lengths, as N_a increases their $dS/d\gamma$ values seem to converge on one common value of 70mV/decade, which is considered as an ideal value of $dS/d\gamma$ ($=S_0$) for a long channel *uniformly-doped* VTCMOS *at* $|V_{bs}| = 1V$. The solid arrows point to the regime of the severe short channel effect. As the channel length and substrate doping concentration decrease, γ decreases but S increases. Consequently, $dS/d\gamma$ decreases. This plot suggests that VTCMOS design should follow the direction where $dS/d\gamma\big|_{Structural\ parameters}$ can be maximized. We have also found from the numerical simulations that γ and S can be expressed by the following empirical equation:

$$S = dS/d\gamma(\gamma - 0.8) + 115 \quad \text{(in the unit of } mV/decade\text{)}. \qquad (10)$$

For the long-channel and 0.1um MOSFET, $dS/d\gamma$ are around 70 and 50 mV/decade, respectively. This equation supports the fact that as $dS/d\gamma$ decreases (worse SCE) S increases with decreasing γ.

Fig 8 shows the relative enhancement of of $I_{on}(a)$ at $\gamma = 0.3$ and at $V_{bs} = 0$, –0.5, and –1V, as a function of $dS/d\gamma$. It is obvious that $I_{on}(a)$ at each V_{bs} increases with increasing $dS/d\gamma$ (suppressed SCE). The three lines represent the slope of $I_{on}(a)$ at $V_{bs} = 0V$. At a larger $dS/d\gamma$, steeper increase of $I_{on}(a)$ with increasing V_{bs} is clearly demonstrated. Important message of this plot is that at a larger $dS/d\gamma$ relative enhancement of $I_{on}(a)$ at a fixed stand-by off current (10^{-13} A/μm) becomes larger as V_{bs} increases. This result confirms that the SCE should be suppressed to maximize $I_{on}(a)$ and thus V_0 should be increased in terms of the SCE in VTCMOS.

5. OPTIMUM DEVICE PARAMETERS

To achieve the best conditions (smaller $I_{off}(s)$ and larger $I_{on}(a)$ or shorter t_{pd}) of the performance of a VTCMOS, the followings are suggested: (i) As seen in Fig 4, the selections of V_{dd} and $|V_{bs}|$ should be made so as to satisfy both short t_{pd} and low P_T requirements. (ii) $|V_{bs}|$ should be set as large as possible to minimize $I_{off}(s)$. However, note that the maximum value of $|V_{bs}|$ is limited by the junction leakage. (iii) As seen in Fig 5, if $|V_{bs}| < |V_0|$ VTCMOS should be designed to have a smaller γ to get larger $I_{on}(a)$, while if $|V_{bs}| > |V_0|$ VTCMOS with a large γ should be utilized. (iv) Finally, VTCMOS should be designed to suppress the SCE to enhance $I_{on}(a)$ and to make a steep reduction of $I_{off}(s)$.

6. CONCLUSION

A very compact analytical VTCMOS model has been developed to facilitate deep-submicron VTCMOS designs for ultra low power applications. Regardless its simplicity, the model is able to explain

and predict the various features of a VTCMOS both in qualitative and quantitative manners. For the first time, the short channel effect on the performance of VTCMOS has been both qualitatively and qualitatively investigated. New parameter, $dS/d\gamma$, is introduced to quantify the SCE. The optimum conditions of a VTCMOS have been discussed with a clear physical background. The compact and predicative VTCMOS model presented here provides low-power circuit designers with a convenient and accurate way to start their advanced circuit design and research.

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