Analysis and Future Trend of Short-Circuit Power

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***Abstract*—A closed-form expression for short-circuit power dissipation of CMOS gates is presented which takes short-channel effects into consideration. The calculation results show good agreement with the SPICE simulation results over wide range of load capacitance and channel length. The change in the short-circuit power, P_S, caused by the scaling in relation to the charging and discharging power, P_D, is discussed and it is shown that basically power ratio, $P_S/(P_D + P_S)$, will not change with scaling if $V_{\rm TH}/V_{\rm DD}$ is kept constant. This paper also handles the short-circuit power of series-connected MOSFET structures which appear in NAND and other complex gates.**

***Index Terms*—Low-power design, power modeling and estimation, simulation, VLSI.**

List of Parameters Used

α	Velocity saturation index.
α_N	Velocity saturation index of NMOS.
α_P	Velocity saturation index of PMOS.
α_{NNJ}	Effective velocity saturation index of N series-connected NMOS structure with Jth NMOS gate from output as an input.
α_{PNJ}	Effective velocity saturation index of N series-connected PMOS structure with Jth PMOS gate from output as an input.
β_r	Beta ratio $(=I_{D0P}/I_{D0N})$
$C_{\rm IN}$	Input node capacitance
$C_{\rm OUT}$	Output load capacitance
C_G	Gate capacitance of inverter
η_P	Power ratio $(=P_S/(P_D + P_S))$.
f	Frequency.
FO	Fanout $(=C_{\rm OUT}/C_{\rm IN})$.
fo	Transistor drivability ratio of succeeding gates.
I_D	Drain current.
I_{DN}	Drain current of NMOS.
I_{DP}	Drain current of PMOS.
I_{D0N}	Saturated drain current of NMOS at $V_{{\rm GS}N} = V_{{\rm DS}N} = V_{\rm DD}$.
I_{D0P}	Saturated drain current of PMOS at $\lvert V_{{\rm GS}P}\rvert = \lvert V_{{\rm DS}P}\rvert = V_{\rm DD}$.
$I_{D0N\,{\rm IN}}$	Saturated drain current of NMOS of previous gate stage.
$I_{D0P\,{\rm IN}}$	Saturated drain current of PMOS of previous gate stage.
L_N	NMOS channel length.
L_P	PMOS channel length.
P_D	Dynamic power dissipation per switching $(=C_{\rm OUT}V_{\rm DD}^2/2)$.
P_S	Short-circuit power dissipation per switching.
t	Time.
t_T	Transition time of input voltage.
τ_N	$=C_{\rm OUT}V_{\rm DD}/I_{D0N}$, transition time of output voltage.
$V_{\rm DD}$	Supply voltage.
V_{D0}	Drain saturated voltage at $V_{{\rm GS}P} = V_{\rm DD}$.
V_{D0P}	Drain saturated voltage of PMOS at $V_{{\rm GS}P} = V_{\rm DD}$.
$V_{\rm DS}$	Drain-source voltage.
$V_{\rm GS}$	Gate-source voltage.
$V_{{\rm GS}P}$	Gate-source voltage of PMOS.
$V_{\rm OUT}$	Output voltage.
$V_{\rm TH}$	Threshold voltage.
$V_{{\rm TH}N}$	Threshold voltage of NMOS.
$V_{{\rm TH}P}$	Threshold voltage of PMOS.
v_{D0P}	Normalized drain saturated voltage of PMOS at $V_{{\rm GS}P} = V_{\rm DD}(=V_{D0P}/V_{\rm DD})$.
$v_{\rm OUT}$	Normalized output voltage $(=V_{\rm OUT}/V_{\rm DD})$.
v_{TN}	Normalized threshold voltage of NMOS $(=V_{{\rm TH}N}/V_{\rm DD})$.
v_{TP}	Normalized threshold voltage of PMOS $(=V_{{\rm TH}P}/V_{\rm DD})$.

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I. Introduction

In recent years, low-power design of CMOS very large scale integrated circuits (VLSIs) draws much attention. The power dissipation of CMOS gates in an active mode consists of two components. One is a dynamic power component, P_D, which corresponds to the charging and discharging of the load capacitance. The other is a short-circuit power component, P_S. Although the first one is well characterized, the short-circuit power or in other words crowbar current power component has not been fully studied. As power dissipation becomes the more serious problem, the more accurate estimation of the power dissipation is needed and in this context, studying P_S is crucial for the future VLSI designs.

Veendrick [1] first reported an expression for P_S but it did not take in account the P_S dependence on load capacitance, $C_{\rm OUT}$, although P_S is a strong function of $C_{\rm OUT}$. In [2], P_S dependence on $C_{\rm OUT}$ was first introduced but it neglected the short-channel effects on P_S. The authors of [3] and [4] then introduced the short-channel effects in P_S through the use of α-power law MOS model [5], but their expressions diverge to infinity when $C_{\rm OUT} = 0$ which is not true in reality, and hence loses reliability when the load capacitance is small. One more drawback is that the expressions include the solution of quadratic or cubic equations so that the expressions are complicated.

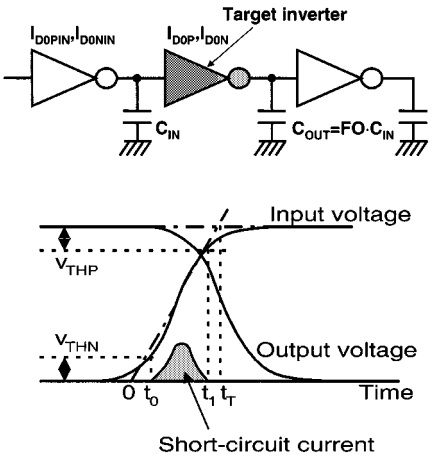

Fig. 1. Voltage waveform of CMOS inverter operation.

In this paper, a closed-form expression is presented which resolves the above-mentioned problems and the future trend of the $P_S/(P_D+P_S)$ is discussed, which answers a long-standing question if the P_S is getting more and more serious or not in the future. The answer is that basically $P_S/(P_D+P_S)$ will not change with scaling if $V_{\rm TH}/V_{\rm DD}$ is kept constant, which will be discussed in detail in Section V. This paper also handles the short-circuit power of series-connected MOSFET structures which appear in NAND and other complex gates, which will be discussed in detail in Section IV.

Section II describes the derivation of the basic formula for the short-circuit power dissipation using α-power law model [5]. In Section III, the calculated results using the formula are compared with SPICE simulation results to show the validity of the formula. In Section IV, the short-circuit power of series-connected MOSFET is derived by introducing effective α for series-connected MOSFETs. In Section V, the future direction of the short-circuit power dissipation is discussed. Section VI introduces the simpler and approximated which will be useful for the easier estimation. Section VII is dedicated to conclusions.

II. Short-Circuit Power Dissipation Formula

Fig. 1 shows the typical input and output voltage waveforms of a CMOS inverter discharging the load capacitance. Although discharging case is described here, the charging case can be treated similarly. t_T is a transient time of the input voltage, t_0 is the time when the input voltage reaches the threshold voltage of NMOS, and t_1 is the time when the input voltage reaches the threshold voltage of PMOS. The short-circuit current flows between t_0 and t_1. When $C_{\rm OUT}$ is sufficiently large, it can be assumed that NMOS operates in the saturated region and PMOS operates in the linear region between t_0 and t_1. With these assumptions, an expression for short-circuit power when the input is very fast, P_S $(t_T \ll \tau_N)$, can be derived as follows:

$$P_S(t_T \ll \tau_N) = 2\frac{I_{D0P}I_{D0N}}{v_{D0P}C_{\rm OUT}}t_T^2 \times \frac{(1-v_{TN}-v_{TP})^{\alpha_P/2+\alpha_N+2}}{(1-v_{TN})^{\alpha_N}(1-v_{TP})^{\alpha_P/2}}\frac{f(\alpha)}{\alpha_N+1} \quad (1)$$

where

$$f(\alpha)=\left\{\frac{1}{\alpha_N+2}-\frac{\alpha_P}{2(\alpha_N+3)}+\frac{\alpha_P}{\alpha_N+4}\left(\frac{\alpha_P}{2}-1\right)\right\}. \quad (2)$$

The detailed derivation of $f(\alpha)$ can be found in Appendix. The expression for a charging case of the load capacitance can be obtained by exchanging N and P suffixes.

This formula, however, suffers from the above-mentioned problem that the P_S diverges to infinity when $C_{\rm OUT}=0$. On the other hand, P_S expression for $C_{\rm OUT}=0$ case, which means that the input rump is slower than the output transition, has been obtained $(P_S(t_T \gg \tau_N))$ as follows [5]:

$$P_S(t_T \gg \tau_N) = V_{\rm DD}t_T I_{D0P}\frac{1}{\alpha_P+1}\frac{1}{2^{\alpha_P}}\frac{(1-v_{TN}-v_{TP})^{\alpha_P+1}}{(1-v_{TP})^{\alpha_P}}. \quad (3)$$

Now, (1) and (3) are combined by taking a harmonic average of the two quantities to build the general formula, P_S, which covers both of the slow and fast input case. The resultant expression for P_S is free from the above-mentioned divergence problem

$$P_S=\frac{1}{\frac{1}{P_S(t_T\ll\tau_N)}+\frac{1}{P_S(t_T\gg\tau_N)}}. \quad (4)$$

Substituting (1) into (4), the short-circuit power dissipation is obtained as follows:

$$P_S=\frac{1}{\frac{v_{D0P}C_{\rm OUT}g(v_T,\alpha)}{2I_{D0P}I_{D0N}t_T^2}+\frac{h(v_T,\alpha)}{V_{\rm DD}t_TI_{D0P}}} \quad (5)$$

where

$$g(v_T,\alpha)=\frac{\alpha_N+1}{f(\alpha)}\frac{(1-v_{TN})^{\alpha_N}(1-v_{TP})^{\alpha_P/2}}{(1-v_{TN}-v_{TP})^{\alpha_P/2+\alpha_N+2}} \quad (6)$$

$$h(v_T,\alpha)=2^{\alpha_P}(\alpha_P+1)\frac{(1-v_{TP})^{\alpha_P}}{(1-v_{TN}-v_{TP})^{\alpha_P+1}}. \quad (7)$$

This formula expresses the P_S in terms of t_T and can be used to estimate the short-circuit power when input transition time is given. In discussing the scaling characteristics of the short-circuit power dissipation, however, it is better to eliminate t_T by replacing t_T with a function of the saturated drain current of the previous gate stage, $I_{D0N\,\rm IN}$, $I_{D0P\,\rm IN}$, and the input node capacitance, $C_{\rm IN}$ [5].

Since the input voltage is the output voltage of another CMOS logic gate, the transient time, t_T, can be expressed as follows [5]:

$$t_T=\frac{C_{\rm IN}V_{\rm DD}}{I_{D0P\,\rm IN}}\left(\frac{0.9}{0.8}+\frac{v_{D0P}}{0.8}\ln\frac{10v_{D0P}}{e}\right)=\frac{C_{\rm IN}V_{\rm DD}}{I_{D0P\,\rm IN}}k(v_{D0P}). \quad (8)$$

Substituting (8) into (5), the short-circuit power dissipation without using t_T is readily obtained as follows:

$$P_S=\frac{k(v_{D0P})V_{\rm DD}^2C_{\rm IN}fo^2}{\frac{v_{D0P}g(v_T,\alpha)}{2k(v_{D0P})}{\rm FO}\beta_r+h(v_T,\alpha)fo} \quad (9)$$

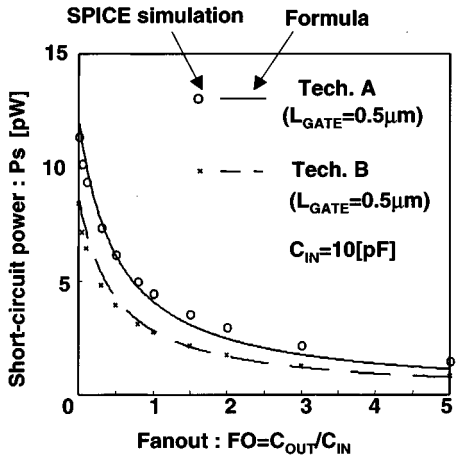

Fig. 2. Short-circuit power dependence on fanout.

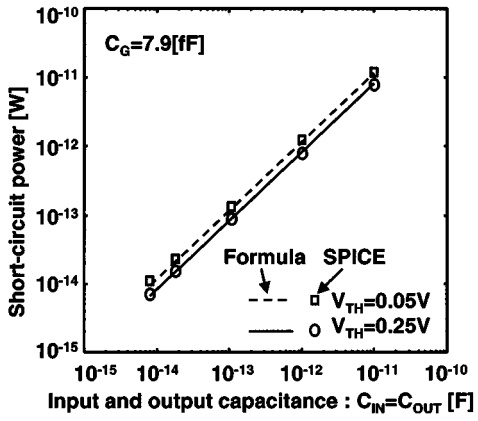

Fig. 3. Short-circuit power dependence on the input and output node capacitance.

TABLE I
SPICE LEVEL3 MOS PARAMETER SETS.

	Tech. A	Tech. B
V_{THN} (V_{BS}=0) [V]	0.55	0.57
V_{THP} (V_{BS}=0) [V]	0.61	0.56
I_{D0}(W_N=10μm) [mA]	0.92	1.8
V_{D0}	0.5	0.5
α_N	1.38	1.6
α_P	1.3	1.6

$$k(v_{D0P}) = \frac{0.9}{0.8} + \frac{v_{D0P}}{0.8} \ln \frac{10 v_{D0P}}{e} \tag{10}$$

$$g(v_T, \alpha) = \frac{\alpha_N + 1}{f(\alpha)} \frac{(1 - v_{TN})^{\alpha_N}(1 - v_{TP})^{\alpha_P/2}}{(1 - v_{TN} - v_{TP})^{\alpha_P/2 + \alpha_N + 2}} \tag{11}$$

$$h(v_T, \alpha) = 2^{\alpha_P}(\alpha_P + 1) \frac{(1 - v_{TP})^{\alpha_P}}{(1 - v_{TN} - v_{TP})^{\alpha_P + 1}} \tag{12}$$

$$\mathrm{FO} = \frac{C_{\mathrm{OUT}}}{C_{\mathrm{IN}}}, \quad fo = \frac{I_{D0P}}{I_{D0P\,\mathrm{IN}}}, \quad \beta_r = \frac{I_{D0P}}{I_{D0N}}. \tag{13}$$

III. Comparison Between Calculated and SPICE Simulation Results

The calculation results by the proposed formula agree well with the SPICE simulation results as shown in Fig. 2. Two completely different MOS model parameter sets are used to show the validity of the formula. The MOS parameter sets are listed in Table I. A CMOS inverter chain shown in Fig. 1 is used for the comparison. In order to confirm the validity of the proposed formulas when the typical load capacitance (fF order) is used, the short-circuit power dependence on the load capacitance (C_{IN} and C_{OUT}) is calculated. Fig. 3 shows the result. FO is set to 1 and C_{IN} and C_{OUT} changes from 7.9 fF (the gate capacitance of the inverter, C_G) to 10 pF. It is seen that the proposed formulas are in good accordance with the SPICE simulation.

In Fig. 4, the SPICE simulation results for the dependence of P_S on FO are compared with the calculation results by the present formula and the previously published Vemuru formula in [3]. The Vemuru formula deviates from the simulation results when the fanout is very small and when the fanout is greater than three. On the other hand, the proposed formula reproduces the simulation results well.

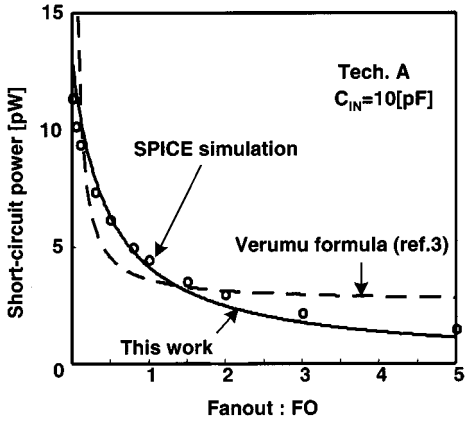

Fig. 4. Comparison between this work and previously published formula.

The dependence of P_S on I_{D0N}, I_{D0P} and α is also compared between SPICE simulation and the present expression. Fig. 5 shows the short-circuit power dependence on PMOS and NMOS drivability ratio, β_r. Again the present formula reproduces the simulation results well. Fig. 6 shows the dependence on the MOSFET channel length, L_N and L_P. Since α is changed when the channel length is changed, Fig. 6 indicates the validity of the short-circuit power dependence on α_N and α_P of the current formula.

IV. Short-Circuit Power Dissipation of Series-Connected MOSFET Structure

So far, the short-circuit power of only a CMOS inverter is considered. In this section, however, the more complicated structure, series-connected MOSFET structure, SCMS, which appears in NAND/NOR gates (see Fig. 7) is investigated. Here, in order to handle the SCMS, the idea in [6] is employed. In [6], in order to derive the delay of the SCMS, the N series-connected MOSFET is replaced by a single MOSFET structure, SMS (see

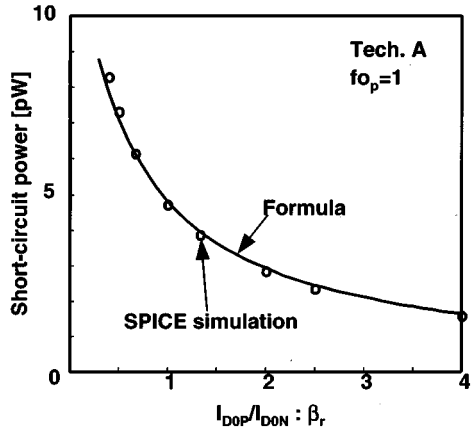

Fig. 5. Short-circuit power dependence on β_r.

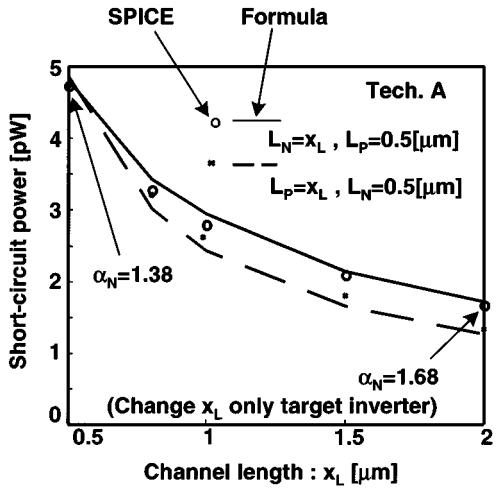

Fig. 6. Short-circuit power dependence on channel length.

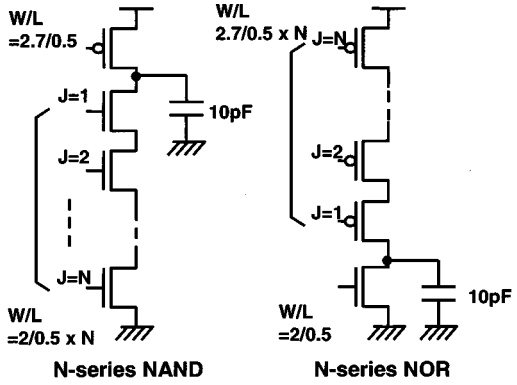

Fig. 7. N series-connected model structure (SCMS).

Fig. 8). A method has been proposed to extract effective parameters, I_{D0NN} (effective I_{D0N} of the SMS), V_{D0}, and α for the SMS. This paper follows the proposed method in [6] to extract I_{D0NN}, and V_{D0} for the SMS but the method to extract the effective α is modified.

As is shown in [6], V_{D0} of the SMS is unchanged from the V_{D0} of one MOSFET in the SCMS, and I_{D0N} is calculated from I_{D0N1} and I_{D0N2} as follows:

$$I_{D0NN} = \frac{I_{D0N1} I_{D0N2}}{(I_{D0N1} - I_{D0N2})(N-1) + I_{D0N2}}. \tag{14}$$

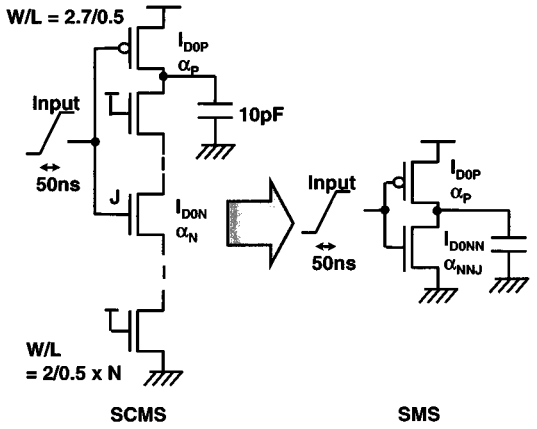

Fig. 8. Approximate N series-connected MOSFETs (SCMS) with single MOSFET structure (SMS).

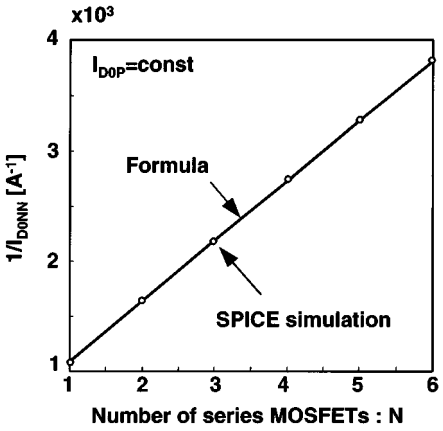

Fig. 9. $1/I_{D0NN}$ dependence on number of series MOSFETs.

The calculated I_{DONN} is shown in Fig. 9 which shows good agreement with the simulation results. On the other hand, α is not so easy to approximate. In this paper, a method to calculate $\alpha_{N(P)NJ}$ formula is proposed using simulated $\alpha_{N(P)11}, \alpha_{N(P)21}$, and $\alpha_{N(P)22}$. $\alpha_{N(P)NJ}$ is effective velocity saturation index of N series-connected N(P)MOS structure with Jth N(P)MOS gate from output as an input.

Scrutinizing the SPICE simulation results, the following empirical formulas can be used for the case of $J = 1$ and $J = N$:

$$\alpha_{NN1} = \frac{\alpha_{N11}\alpha_{N21}}{(\alpha_{N11} - \alpha_{N21})\frac{\ln N}{\ln 2} + \alpha_{N21}}$$
$$\alpha_{PN1} = \frac{\alpha_{P11}\alpha_{P21}}{(\alpha_{P11} - \alpha_{P21})\frac{\ln N}{\ln 2} + \alpha_{P21}} \tag{15}$$
$$\alpha_{NNN} = \frac{\alpha_{N11}\alpha_{N22}}{(\alpha_{N11} - \alpha_{N22})(N-1) + \alpha_{N22}}$$
$$\alpha_{PNN} = \frac{\alpha_{P11}\alpha_{P22}}{(\alpha_{P11} - \alpha_{P22})\frac{\ln N}{\ln 2} + \alpha_{P22}}. \tag{16}$$

A comparison of the calculated αs with the simulation results is shown in Fig. 10(a) and (b).

Fig. 11 shows the short-circuit power comparison of the SCMS between the calculation and simulation. The calculation results can be favorably compared with the simulation. Once

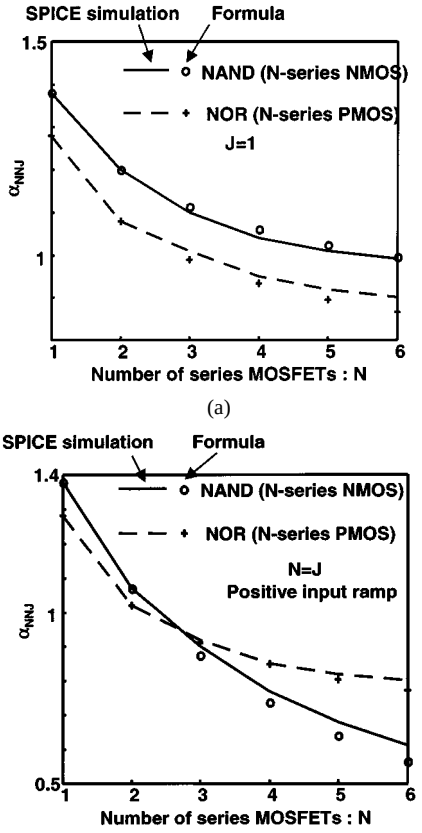

Fig. 10. α_{NNJ} dependence on number of series MOSFETs (a) $J = 1$ (b) $J = N$.

α_{NNJ} and α_{PNJ} are obtained, the general N and J can be obtained using the following formula:

$$\alpha_{NNJ} = \alpha_{NN1} + \frac{(\alpha_{NNN} - \alpha_{NN1})(J-1)}{(N-1)}$$
$$\alpha_{PNJ} = \alpha_{PN1} + \frac{(\alpha_{PNN} - \alpha_{PN1})(J-1)}{(N-1)}. \quad (17)$$

V. The Change of the Short-Circuit Power Dissipation with Scaling

Now, let us consider the power ratio, $\eta_P = P_S/(P_D+P_S)$, to investigate the impact of the short-circuit power. It is straightforward to obtain the power ratio η_P knowing that P_D is expressed as $C_{\rm OUT}V_{\rm DD}^2/2$. Figs 12 and 13 show comparisons of η_P between calculation and simulation. The dependence of η_P on the threshold voltage and the supply voltage is well reproduced over a wide range of $V_{\rm TH}$ and $V_{\rm DD}$ by the present formula. It is seen from the figures that $P_S/(P_D + P_S)$ is about 10% for a typical design. This means that the contribution of the short-circuit power to the total active power is about 10%.

Can η_P be changed over time? η_P is a function of α, fanout, $V_{\rm TH}/V_{\rm DD}$ and $I_{D0\,\rm OUT}/I_{D0\,\rm IN}$ as shown in the following formula:

$$\eta_P = \frac{P_s}{P_D+P_S} = \frac{1}{\frac{v_{D0P}g(v_T,\alpha)}{4k^2(v_{D0P})}\left(\frac{\rm FO}{fo}\right)^2\beta_r + \frac{h(v_T,\alpha)}{2k(v_{D0P})}\frac{\rm FO}{fo}+1}. \quad (18)$$

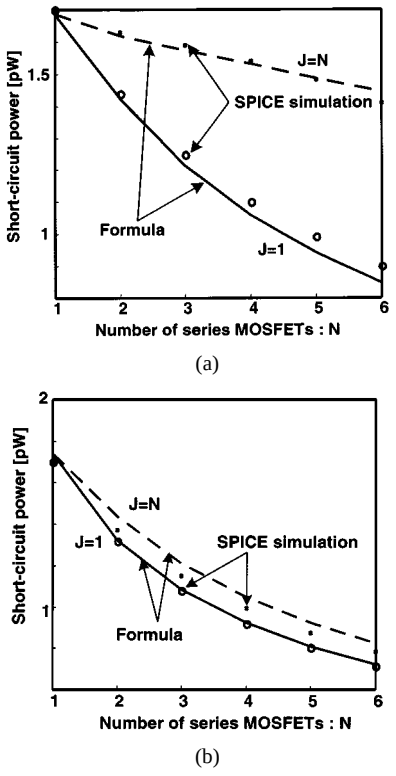

Fig. 11. Short-circuit power dependence on number of series MOSFETs (a) N-series NAND (b) N-series NOR.

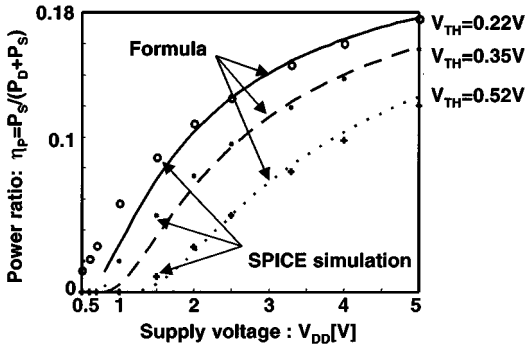

Fig. 12. Power ratio dependence on supply voltage.

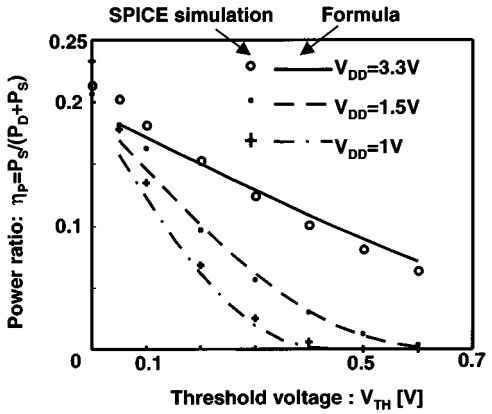

Fig. 13. Power ratio dependence on threshold voltage.

The fanout and $I_{D0\,\rm OUT}/I_{D0\,\rm IN}$ are essentially unchanged if the design style is unchanged even if the device is shrunk. α is

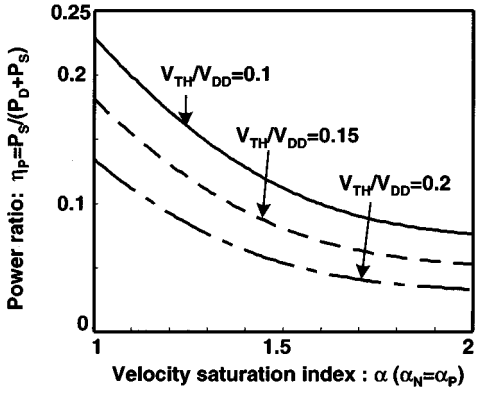

Fig. 14. Power ratio dependence on α.

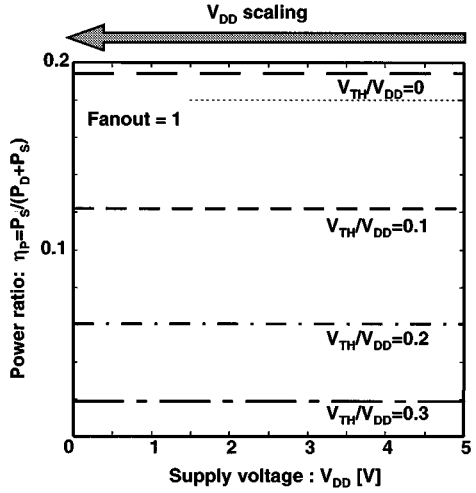

Fig. 15. Power ratio dependence on $V_{\rm DD}$ scaling.

not a strong function of a device scaling (see Fig. 14). Equation (18) shows that if $V_{\rm TH}/V_{\rm DD}$ is constant, η_P remains constant even though the $V_{\rm DD}$ is scaled. In order to confirm the validity of this result, η_P dependence on $V_{\rm DD}$ scaling is shown in Fig. 15. Considering the tendency that $V_{\rm TH}/V_{\rm DD}$ will be slightly increasing to keep the standby power in a tolerant level when the supply voltage is decreased as device miniaturization proceeds, the importance of the short-circuit power will not be increased (see Fig. 16).

VI. Simplified Formula for Short-Circuit Power

If the precision is of importance in estimating the short-circuit power, (9) is to be used but if the dependence on various parameters is of interest, the simpler expression is of use. In this section, the simpler but less accurate formula is presented so as to give insight in the parametric dependence of the short-circuit power.

First, v_{D0} can be fixed at 0.5, v_{TN} and v_{TP} are both set equal to v_T and α_N and α_P are both set to α without much degradation in accuracy. Then, the following expressions are obtained:

$$P_S(t_T \ll \tau_N) = \frac{10}{3}\frac{(0.5-v_T)^3}{\alpha^2 2^{3v_T^2}} C_{\rm IN} V_{\rm DD}^2 \frac{fo^2}{{\rm FO}\beta_r} \quad (19)$$

$$P_S(t_T \gg \tau_N) = \frac{(0.5-v_T)^{3/2}}{10\cdot 2^{3v_T+2\alpha}} C_{\rm IN} V_{\rm DD}^2 fo. \quad (20)$$

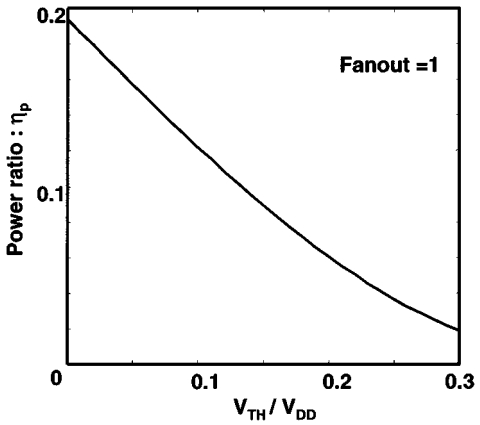

Fig. 16. Power ratio dependence on $V_{\rm TH}/V_{\rm DD}$.

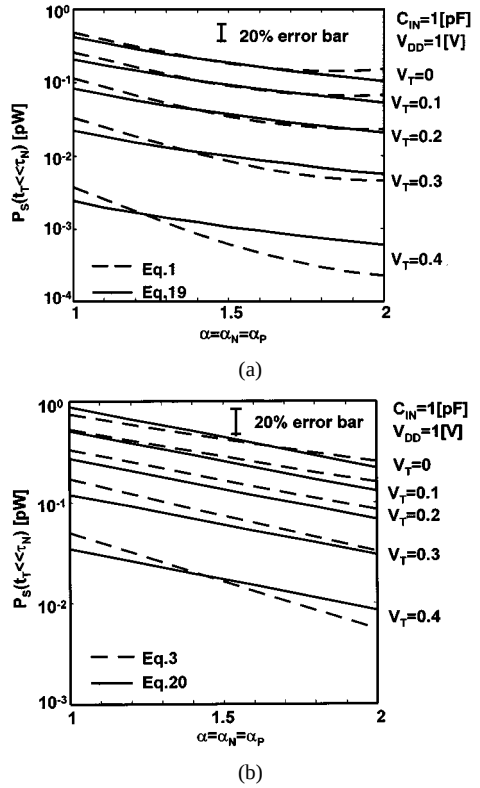

Fig. 17. Comparison between (1) and (3) and simple formula (19) and (20): (a) (1) and (19); (b) (3) and (20).

As is seen from Fig. 17, the relative error of the expression compared with the (1) and (3) is less than 20% in the range of $0 \le v_T \le 0.4$ and $1 \le \alpha \le 2$. When $v_T \ge 0.5$, the short-circuit current does not flow at all. It is easily seen from these formulas that the short-circuit power monotonically increases as α decreases, as fanout decreases and as the ratio of the threshold voltage over $V_{\rm DD}$ decreases.

VII. Conclusion

A simple and closed-form formula for the short-circuit power dissipation is derived which correctly reproduces the dependence on various parameters such as the threshold voltage, the supply voltage, beta ratio, transition time of input voltage, load capacitance, and input capacitance. The formula includes the

short-channel effects through a velocity saturation index (α) of the α-power law MOSFET model. The formula can be used to estimate the short-circuit power dissipation with more accuracy than the previously published formulas.

By rewriting the formula using fanout and by eliminating the transition time of the input voltage, the scaling characteristics of the short-circuit power is discussed. If the ratio of $V_{\rm TH}/V_{\rm DD}$ is constant, the ratio of the short-circuit power vs. the dynamic power will remain constant even though the $V_{\rm DD}$ is scaled.

It has been shown that the formula is effective not only for CMOS inverters but also for the more complex CMOS gates such as NORs and NANDs. This is achieved by using effective single MOS structure approximation.

It is shown that the short-circuit power monotonically increases as α decreases, as fanout decreases and as the ratio of the threshold voltage over $V_{\rm DD}$ decreases. In order to design low-power, high-speed CMOS VLSIs, a low threshold voltage is sometimes used to achieve sufficient drivability in a low $V_{\rm DD}$ regime. In this case, the effect of the short-circuit power dissipation will increase and become an important part (up to 20%) of the total power dissipation of CMOS VLSIs.

APPENDIX

In the α-power law model, the drain current I_D is given as follows [6]:

$$I_D = \begin{cases} 0, & \text{(cutoff region)} \\ I'_{D0}\left(2 - \dfrac{V_{\rm DS}}{V'_{\rm DS}}\right)\dfrac{V_{\rm DS}}{V'_{\rm DS}}, & \text{(linear region)} \\ I'_{D0}, & \text{(saturated region)} \end{cases} \tag{A1}$$

where

$$I'_{D0} = I_{D0}\left(\frac{V_{\rm GS} - V_{\rm TH}}{V_{\rm DD} - V_{\rm TH}}\right)^{\alpha} \tag{A2}$$

$$V'_{D0} = V_{D0}\left(\frac{V_{\rm GS} - V_{\rm TH}}{V_{\rm DD} - V_{\rm TH}}\right)^{\alpha/2}. \tag{A3}$$

When $\alpha = 2$, this model becomes the Shockley model.

In this Appendix, the CMOS inverter shown in Fig. 1 is used for the derivation of the short-circuit power dissipation. Fig. 1 shows the input and output voltage waveform discharging the load capacitance. Where t_T is the transient time of the input voltage, t_0 is the time when input voltage reach at the threshold voltage of NMOS, and t_1 is the time when input voltage reach at the threshold voltage of PMOS. The short-circuit current flows between t_0 and t_1. Then, the output voltage is governed by the following differential equation:

$$C_{\rm OUT}\frac{dV_{\rm OUT}}{dt} = I_{DP} - I_{DN}. \tag{A4}$$

When $t_T \ll \tau_N$, however, it can be assumed that $I_{DP} \ll I_{DN}$. When the transient time of the input is slower than τ_N, it can be assumed that NMOS is in the saturated region between t_0 and t_1. Then, (A4) can be rewritten as

$$C_{\rm OUT}\frac{dV_{\rm OUT}}{dt} = -I_{D0N}\left(\frac{V_{{\rm GS}N} - V_{{\rm TH}N}}{V_{\rm DD} - V_{{\rm TH}N}}\right)^{\alpha_N} \tag{A5}$$

which should be solved with the initial condition, $V_{\rm OUT} = V_{\rm DD}$. Solving the above differential equation, we have

$$v_{\rm OUT}(t) = 1 - \frac{1}{\tau_N(\alpha_N+1)}\frac{(t - t_T v_{TN})^{\alpha_N+1}}{(t_T - t_T v_{TN})^{\alpha_N}}. \tag{A6}$$

In this condition when $t_T \ll \tau_N$, PMOS is in the linear region. From (A1), (A2), and (A3), the PMOS drain current, I_{DP}, is calculated as

$$I_{DP} = 2\frac{I_{D0P}}{V_{D0P}}\left(\frac{|V_{{\rm GS}P}| - V_{TP}}{V_{\rm DD} - V_{TP}}\right)^{\alpha_P/2} \times V_{{\rm DS}P} - \frac{I_{D0P}}{V_{D0P}^2}V_{{\rm DS}P}^2. \tag{A7}$$

Since the output capacitance is relatively large, the output voltage moves very slowly. Then, $V_{{\rm DS}P}$ is small when the input is changing and with this assumption, the second term of (A7) can be ignored. The second term of (A6) becomes $v_{{\rm DS}P}$, (A7) can be solved in terms of I_{DP}. From these formulas, the short-circuit power dissipation, P_S, is shown as

$$\begin{aligned} &P_S(t_T \ll \tau_N) \\ &\quad = V_{\rm DD}\int_{t_0}^{t_1} I_{DP}\,dt \\ &\quad = \frac{2V_{\rm DD}I_{D0P}t_T}{v_{D0P}\tau_N(\alpha_N+1)(1-v_{TN})^{\alpha_N}(1-v_{TP})^{\alpha_P/2}} \\ &\qquad \times \int_{t_0}^{t_1}\left(1 - \frac{t}{t_T} - v_{TP}\right)^{\alpha_P/2}\left(\frac{t}{t_T} - v_{TN}\right)^{\alpha_N+1} dt. \end{aligned} \tag{A8}$$

Note that

$$\begin{aligned} &\int_{t_0}^{t_1}\left(1 - \frac{t}{t_T} - v_{TP}\right)^{\alpha_P/2}\left(\frac{t}{t_T} - v_{TN}\right)^{\alpha_N+1} dt \\ &\quad = \int_0^{1-v_{TP}-v_{TN}} \{(1 - v_{TN} - v_{TP}) - x\}^{\alpha_P/2} \\ &\qquad \times x^{\alpha_N+1} t_T\,dx \end{aligned} \tag{A9}$$

where $x = (t/t_T) - v_{TN}$. Now, the Taylor transformation is applied for the integrand

$$\begin{aligned} &\{(1 - v_{TN} - v_{TP}) - x\}^{\alpha_P/2} \\ &\quad = m^{\alpha_P/2} - \alpha_P/2 m^{\alpha_P/2-1}x \\ &\qquad + \frac{1}{2}\cdot\frac{\alpha_P}{2}\left(\frac{\alpha_P}{2} - 1\right)m^{\alpha_P/2-2}x^2 - \cdots \end{aligned} \tag{A10}$$

where $m = 1 - v_{TN} - v_{TP}$. Then the integration can be carried out as follows:

$$\begin{aligned} t_T m^{\alpha_P/2+\alpha_N+2}\Bigg\{&\frac{1}{\alpha_N+2} - \frac{\alpha_P}{2(\alpha_N+3)} \\ &+ \frac{\alpha_P}{2\cdot 2(\alpha_N+4)}\left(\frac{\alpha_P}{2} - 1\right) - \cdots\Bigg\}. \end{aligned} \tag{A11}$$

Let us concentrate on the quantity in the parenthesis. When the third term is multiplied by 4, a good appropriation can be obtained which fits well with SPICE simulation and this accounts

for the higher terms than the fourth. Hence, the quantity in the parenthesis can be approximated as $f(\alpha)$, which is defined as

$$f(\alpha) = \left\{ \frac{1}{\alpha_N + 2} - \frac{\alpha_P}{2(\alpha_N + 3)} + \frac{\alpha_P}{\alpha_N + 4} \left(\frac{\alpha_P}{2} - 1 \right) \right\}. \tag{A12}$$

With $f(\alpha)$, (1) in the text can be easily derived.

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