LSI design toward 2010 and low-power technology

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Biography

Takayasu Sakurai received the B.S., M.S. and Ph.D degrees in EE from University of Tokyo, Japan, in 1976, 1978, and 1981, respectively. In 1981 he joined Toshiba Corporation, where he designed CMOS DRAM, SRAM and BiCMOS ASIC’s. He also worked on interconnect delay and capacitance modeling known as Sakurai model and alpha power-law MOS model. From 1988 through 1990, he was a visiting researcher at Univ. of Calif., Berkeley, doing research in the field of VLSI CAD. From 1990 back in Toshiba, he managed RISCs, media processors and MPEG2 LSI designs. From 1996, he is a professor at the Institute of Industrial Science, University of Tokyo, working on low-power and high-performance system LSI designs. Prof. Sakurai served as a conference chair for Symposium on VLSI Circuits, a vice chair for ASPDAC and a program committee member for ISSCC, CICC, DAC, ICCAD, FPGA workshop, ISLPED, TAU, and other international conferences. He is also consulting to US startup companies.

Summary:

If we look into the scaling law carefully, we find that three crises can be stringent in realizing LSI’s of the year 2010: namely power crisis, interconnection crisis, and complexity crisis.

As for power crisis, there are activities to lower the power consumption from device level, circuit level to system level. Lowering supply voltage ($V_{DD}$) is very effective in reducing the power but the threshold voltage ($V_{TH}$) should be reduced at the same time for high-speed operation. The low $V_{TH}$, however, increases the leakage current. To overcome this situation, $V_{TH}$ and $V_{DD}$ control through the use of multiple $V_{TH}$, variable $V_{TH}$, multiple $V_{DD}$ and variable $V_{DD}$ are intensively pursued and some have been productized. At the system level, a system LSI approach is promising for realizing low power. The new trend is to exploit cooperation of software and hardware. In the sub 1-volt design, watch out for the abnormal temperature dependence of drain current.

The interconnection will be determining cost, delay, power, reliability and turn-around time of the future LSI’s rather than MOSFET’s. RC delay problem can be solved through LSI architecture realizing “the further, the less communication” with the help of local memories.

It is just impossible to design LSI’s with 100 million transistors from scratch. The complexity issue can only be solved by the sharing and re-use of design data. So-called IP-based design will be preferable. The virtual components are put together on a silicon to build billion transistor LSI’s, which can be compared to the present system implementation with pre-manufactured LSI components.

In the year 2012, sensors / actutors can be integrated on a chip with 0.06µm 2G Si FET’s with $V_{TH}$ & $V_{DD}$ control. Globally asynchronous LSI’s with locally synchronous 10GHz clock will be implemented.
LSI Design Toward 2010 and Low-Power Technology

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1. Scaling and three crises
2. Power crisis
3. Interconnection crisis
4. Complexity crisis

Fig. 1 Title

Fig. 2 Scaling law

Fig. 3 Limit of miniaturization

Fig. 4 Scaling law

Fig. 5 Three crises in VLSI designs

Fig. 6 Ever increasing VLSI power

Scaling Law

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Numbers are exponent to k (k n)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage</td>
<td>a x V^k</td>
</tr>
<tr>
<td>Tr. size</td>
<td>-1</td>
</tr>
<tr>
<td>Gate-thickness</td>
<td>k</td>
</tr>
<tr>
<td>Current</td>
<td>b x V^(1-k)</td>
</tr>
<tr>
<td>Tr. capacitance</td>
<td>c x V^(1-k)</td>
</tr>
<tr>
<td>Tr. delay</td>
<td>d x V^(1-k)</td>
</tr>
<tr>
<td>Tr. power</td>
<td>e x V^(1-k)</td>
</tr>
<tr>
<td>Tr. density</td>
<td>f x V^(1-k)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Interconnection</th>
<th>Length</th>
<th>Width</th>
<th>Thickness</th>
<th>Height</th>
<th>Resistance</th>
<th>Capacitance</th>
<th>Delay/T. delay</th>
<th>Current density</th>
<th>Do. size</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>-1</td>
<td>1.85</td>
<td>1.65</td>
<td>-0.65</td>
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</table>

<table>
<thead>
<tr>
<th>Power crisis</th>
<th>Interconnection crisis</th>
<th>Complexity crisis</th>
</tr>
</thead>
<tbody>
<tr>
<td>Favorable effects</td>
<td>Unfavorable effects</td>
<td></td>
</tr>
<tr>
<td>Size</td>
<td>Power</td>
<td></td>
</tr>
<tr>
<td>Voltage</td>
<td>x1/2</td>
<td></td>
</tr>
<tr>
<td>Electric Field</td>
<td>x1</td>
<td></td>
</tr>
<tr>
<td>Speed</td>
<td>x2</td>
<td></td>
</tr>
<tr>
<td>Cost</td>
<td>x1/4</td>
<td></td>
</tr>
<tr>
<td>Power</td>
<td>x1.6</td>
<td></td>
</tr>
<tr>
<td>RC delay</td>
<td>x3.6</td>
<td></td>
</tr>
<tr>
<td>Current density</td>
<td>x1.8</td>
<td></td>
</tr>
<tr>
<td>Voltage noise</td>
<td>x2.5</td>
<td></td>
</tr>
<tr>
<td>Design complexity</td>
<td>x4</td>
<td></td>
</tr>
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</table>

Fig. 6 Ever increasing VLSI power

(T. Sakurai)
VDD, Power and Current Trend

Fig. 7 VDD, power and current trend

Necessity for Low-Power Design

<table>
<thead>
<tr>
<th>Power range</th>
<th>Concerns</th>
<th>Typical applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt; 0.1W</td>
<td>Battery life</td>
<td>Portable, PDA, Communications</td>
</tr>
<tr>
<td>~ 1W</td>
<td>Inexpensive package limit</td>
<td>Consumer, Set-Top-Box, Audio-Visual</td>
</tr>
<tr>
<td>&gt; 10W</td>
<td>Ceramic package limit</td>
<td>Processor, High-end MPU’s, Multimedia DSP’s</td>
</tr>
</tbody>
</table>

Fig. 8 Necessity of low-power design

What sets the technology trend?

- NMOS ➡️ CMOS  
  Cost up
- Bipolar ➡️ CMOS  
  Speed down
- Not cost nor speed but power set the technology trend.
- Integration can achieve low cost and high speed as a system.

Fig. 9 What sets the technology trend?

Expression for CMOS Power

\[ P = \alpha C_L V_s^2 + \beta I_{DD} \]

- \( \alpha \): Switching probability
- \( C_L \): Load capacitance
- \( V_s \): Signal swing

Fig. 10 Expression for CMOS power

Voltage waveform of CMOS inverter

Fig. 11 Voltage waveform of CMOS inverter

Short-circuit power dissipation formula

\[ P_s = \frac{k(\frac{V_{DD}}{2})f_o^2C_iN V_{DD}^2}{2k(\frac{V_{DD}}{2})} \]

\[ f_o = \frac{C_{OUT}}{C_{IN}} \text{(Fanout)} \]

Fig. 12 Short-circuit power dissipation formula
Comparison between proposed formula and other formula

- Verumu et al’s formula deviates from SPICE simulation
- fanout > 3
- fanout is small (diverge to infinity)

Fig. 13 Comparison between proposed formula and other formulas

The change of the short-circuit power dissipation with scaling

- $P = \alpha f C V_{DD}$ + leakage (sub-Vth, gate, D/S)

Low-voltage
- Variable-$V_{TH}$, multi-$V_{DD}$
  (Super-Cut-off CMOS, dynamic leakage cut-off SRAM, positive temp. coeff., d-type CMOS, optimum voltages)
- Variable-$V_{DD}$, multi-$V_{DD}$
  (Software control)

Low-swing
- Bus, clock, interconnection
  (Reduced Clock Swing F/F, bus with sense-amp. F/F, low-power repeater insertion)

Others
- Easy library generation for early adoption of new tech.
- Micro IDDQ test

Fig. 16 Voltage dependent gate capacitance effect

Solving power issues

Power and delay

$P = \alpha f C V_{DD}$ + leakage (sub-Vth, gate, D/S)

Power : $P = P_{OFF} C_{OX} V_{DD}^2 + I_{OFF} \cdot V_{DD}$

$\text{Delay} = \frac{k \cdot Q}{I}$

$\text{Power} : P = R_{CL} C_{OX} V_{DD}^2 + I_{OFF} \cdot V_{DD}$

$\text{Delay} = \frac{k \cdot Q}{I}$

Fig. 17 Solving power issues

Voltage dependent gate cap. effect

Fig. 15 Voltage dependent gate capacitance effect

Fig. 18 Power and delay
**Concept of Super Cut-off CMOS (SCCMOS)**

- St'by: \( V_{DD} + 0.4V \)
- Active: \( V_{SS} \)
- Low-\( V_{TH} \) cut-off MOSFET
- Low-\( V_{TH} \) logic circuit
- Virtual \( V_{DD} \)
- pMOS insertion case


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**Fig. 19** Concept of super cut-off CMOS

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**Super Cut-off CMOS Scheme (SCCMOS)**

- 0.3µm, triple-metal CMOS process
- \( V_{TH} = 0.2V \)
- 100x100µm² pumping
- freq=10kHz
- 0.1µA (@\( V_{DD} = 0.5V \))

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**Fig. 20** Super cut-off CMOS scheme

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**Delay characteristics (inverter & NAND)**

- \( SCCMOS \):
  - 0.2V \( V_{TH} \) circuit with 0.2V \( V_{TH} \) cut-off MOSFET
  - F.O.=3
- \( MTCMOS \):
  - 0.2V \( V_{TH} \) circuit with 0.6V \( V_{TH} \) cut-off MOSFET
- Conventional
- All 0.6V circuit
- No cut-off MOSFET

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**Fig. 21** Delay characteristics of SCCMOS

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**Losing information in standby**

- System level solution: → Using scan-path flip-flops
- Circuit level solution:

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**Fig. 22** Losing information in standby

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**Dynamic Leakage Cut-off**

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**Fig. 23** Dynamic leakage cut-off SRAM

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**Leakage Reduction of DLC SRAM**

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**Fig. 24** Leakage reduction of DLC SRAM

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T. Sakurai

Power Distribution in CMOS LSI's

Fig. 25 Power distribution in CMOS LSI's

Reduced Clock Swing Flip-Flop

Fig. 26 Reduced clock swing flip-flop

Positive temp. coeff. in low-voltage

Fig. 27 Positive temperature coefficient in low-voltage region

Cause of positive temp. dependence of I_DS

- α-power law model

\[ I_{DS} \propto \mu(T) \left( V_{DD} - V_{TH}(T) \right)^{\alpha} \]

\[ \mu(T) = \mu(T_0) \left( \frac{T}{T_0} \right)^m \]

\[ V_{TH}(T) = V_{TH}(T_0) - \kappa \left( T - T_0 \right) \]

Typical Value: \( \alpha = 1.5 \), \( m = 1.5 \), \( \kappa = 2.5 \text{[mV/T]} \)

Effects of \( V_{TH} \) and \( \mu \) on \( I_{DS} \) when temp. goes up 100[K]

\[ V_{DD}=2.5V, V_{TH}=0.5V \]

\( 10\% \) 35%

\[ V_{DD}=1.0V, V_{TH}=0.2V \]

55% 35%

D-type CMOS

Fig. 29 D-Type CMOS

SOI Processors in ISSCC'99

Fig. 30 SOI processors in ISSCC'99
Hi-Speed is Low-Power

![Energy of various operation](image)

Integration (system LSI) is the key to low-power

<table>
<thead>
<tr>
<th>Operation</th>
<th>Energy/Op (pJ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Add</td>
<td>7</td>
</tr>
<tr>
<td>3-2 Add</td>
<td>2</td>
</tr>
<tr>
<td>Multiply</td>
<td>40</td>
</tr>
<tr>
<td>Latch</td>
<td>1.8</td>
</tr>
<tr>
<td>Internal read</td>
<td>36</td>
</tr>
<tr>
<td>Internal write</td>
<td>71</td>
</tr>
<tr>
<td>I/O</td>
<td>80</td>
</tr>
<tr>
<td>External memory</td>
<td>16000</td>
</tr>
</tbody>
</table>


Example of MPEG2 decoding

- Processor (software) ~25W
- DSP ~4W
- Dedicated system LSI (SW/HW) ~0.7W

Software feedback loop for low-power

Homogeneous vs. Heterogeneous

<table>
<thead>
<tr>
<th>Homogeneous Architecture</th>
<th>Heterogeneous Architecture</th>
</tr>
</thead>
<tbody>
<tr>
<td>(High flexibility)</td>
<td>(Low-power, more efficient)</td>
</tr>
</tbody>
</table>

DRAM Embedding


Two orders of magnitude improvement in bandwidth and power

From URL: www.erniefernandez.com/html/soi.html
Compact yet High-Performance (CyHP)
Library for Low-Power Technologies

11-CELL CyHP LIBRARY

- Library A
- Library B
- Library C

Flip-Flops
- D-FF x1, D-FF x2

Inverters
- INV x1, INV x2, INV x4

Primitive gates
- 2-NAND x2
- 2-NOR x2
- 2-XNOR x1

Compound gates
- 2-INVAND x2
- 2-InvNOR x2

Multiplexers
- 2-MUXinv x1

Number of cells

Fig.38 Compact cell library for quick TAT

Interconnect determines cost & perf.

P: Power, D: Delay, A: Area, T: Turn-around

Fig.40 Interconnect determines cost & performance

Interconnect parameters trend

Year

Fig.41 Interconnect parameters trend

Lorentz Force MOS for micro IDDQ test

Fig.39 Lorentz force MOS for micro IDDQ test

RC delay and gate delay

Year

Fig.42 RC delay and gate delay
Delay and Power Optimization for Repeaters

- **Without Repeaters:**
  - Interconnect delay (ns)
  - Interconnect length (cm)

- **With Repeaters:**
  - Interconnect delay (ns)
  - Interconnect length (cm)

**Delay optimized**
- P: P(repeater) = 0.60 P(interconnect)
- D: 1.09 Dopt

**Power-Delay optimized**
- P: P(repeater) = 0.26 P(interconnect)
- PD: 0.86 of Dopt case

**Power-Delay**

![Graph comparing delay and power optimization with and without Repeaters.](image)

*Fig. 43 Delay and power optimization for Repeaters*

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Capacitive Coupling Noise

- **C12/C20**
- **peak couple noise / signal voltage**

![Graph showing capacitive coupling noise ratio over years.](image)

*Fig. 46 Capacitive coupling noise*

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Coupling noise in RC bus

- **Use of local memories**
- **Difficulty in checking setup and hold time.**

![Graph showing coupling noise in RC bus.](image)

*Fig. 47 Coupling noise in RC bus*

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Locality in space & time

- **Latency**
  - 3ns
- **Throughput**
  - 3ns

![Graph showing locality in space and time.](image)

*Fig. 45 Locality in space and time*

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Coupling among Interconnection

- **0.1μm space**
- **Length 3mm**
- **In-phase**
  - 0=1 0=1 0=1
- **Out-phase**
  - 1=0 0=1 1=0

![Graph showing coupling among interconnections.](image)

*Fig. 48 Coupling among interconnections*
**Interconnect Cross-Section and Noise**

Unscaled / anti-scaled
- Clock
- Long bus
- Power supply

Scaled interconnect
- Signal

1V 15W -> 15A current
5% noise -> 0.05V noise -> 3mΩ sheet R -> 10µm thick Al
Area pad + package, or thick layer on board is needed.

![Interconnect Cross-Section and Noise](image)

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**Overcome complexity crisis**

System LSI: Re-use and sharing

- MPU Core
- Proprietary Logic
- ROM
- RAM
- MPEG Core
- Cache
- USB Core

IP : CPU, DSP, memories, analog, I/O, logic..
HW/FW/SW

![Overcome complexity crisis](image)

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**Skin Effects for Signal Lines**

![Skin Effects for Signal Lines](image)

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**Inductive Effects**

![Inductive Effects](image)

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**Summary**

- Scaling law indicates power, interconnection and complexity crises.
- Low-voltage + threshold control and less-waste design for low-power
- Process, design guidelines and local memory for interconnection issues
- Design reuse and sharing + software programmability for complexity

![Summary](image)