Closed-Form Expressions for Short-Circuit Power of Short-Channel CMOS Gates and its Scaling Characteristics

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***Abstract*- A closed-form expression for short-circuit power dissipation of CMOS gates is presented which takes short-channel effects into consideration. The calculation results show good agreement with the SPICE simulation results over wide range of load capacitance. The change in the short-circuit power, P_S, caused by the scaling in relation to the charging and discharging power, P_D, is discussed and it is shown that basically $P_S / (P_D + P_S)$ will not change with scaling if V_{TH} / V_{DD} is kept constant.**

I. Introduction

In recent years, low-power design of CMOS VLSI's draws much attention. The power dissipation of CMOS gates in an active mode consists of two components. One is a dynamic power component, $P_D = (p_t f C_L V_{DD}^2)$, which corresponds to the charging and discharging of the load capacitance. The other is a short-circuit power component, P_S. Although the first one is well characterized, the short-circuit power or in other words crowbar current power component has not been fully studied. As power dissipation becomes the more serious problem, the more accurate estimation of the power dissipation is needed and in this context, studying P_S is crucial for the future VLSI designs.

Veedrick [1] first reported an expression for P_S but it did not take in account the P_S dependence on load capacitance, C_L, although P_S is a strong function of C_L. In [2], P_S dependence on C_L was first introduced but it neglected the short-channel effects on P_S. Papers [3] then introduced the short-channel effects in P_S through the use of α-power law MOS model [4], but their expressions diverge to infinity when C_L=0 which is not true in reality, and hence loses reliability when the load capacitance is small. One more drawback is that the expressions include the solution of quadratic or cubic equations so that the expressions are complicated.

In this paper, a closed-form expression is presented which resolves the above-mentioned problems and the future trend of the $P_S / (P_D + P_S)$ is discussed for the first time, which answers a long-standing question if the P_S is getting more and more serious or not in the future. The answer is that basically $P_S / (P_D + P_S)$ will not change with scaling if V_{TH} / V_{DD} is kept constant, which will be discussed in detail in Section IV in this paper.

II. Short-Circuit Power Dissipation Formula

Figure 1 shows the typical input and output voltage waveforms of a CMOS inverter discharging the load capacitance. Although discharging case is described here, the charging case can be treated similarly. t_T is a transient time of the input voltage, t_0 is the time when the input voltage reaches the threshold voltage of NMOS, and t_1 is the time when the input voltage reaches the threshold voltage of PMOS. The short-circuit current flows between t_0 and t_1. When C_{OUT} is sufficiently large, it can be assumed that NMOS operates in the saturated region and PMOS operates in the linear region between t_0 and t_1. With these assumptions, an expression for short-circuit power when the input is very fast, $P_S (t_T \ll \tau_N (=C_{OUT}V_{DD}/I_{D0N}))$, can be derived as follows. In this paper, just for simplicity, a number of switching per second is assumed to be 1 and if it is f, all P's should be multiplied by f but the main results of the paper is unchanged.

$$P_S(t_T \ll \tau_N) = 2\frac{I_{D0P}I_{D0N}}{v_{D0P}C_{OUT}} t_T^2 \frac{(1-v_{TN}-v_{TP})^{\frac{\alpha_P}{2}+\alpha_N+1}}{(1-v_{TN})^{\alpha_N}(1-v_{TP})^{\alpha_P/2}} \frac{f(\alpha)}{\alpha_N+1}, \quad (1)$$

where

$$f(\alpha) = \left\{ \frac{1}{\alpha_N+2} - \frac{\alpha_P}{2(\alpha_N+3)} + \frac{\alpha_P}{\alpha_N+4}\left(\frac{\alpha_P}{2}-1\right) \right\}. \quad (2)$$

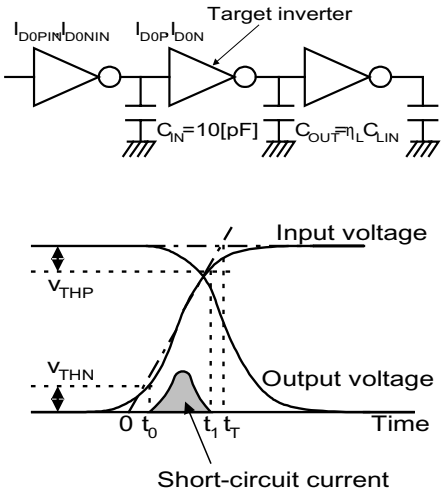

Fig.1 Voltage waveform of CMOS inverter operation

The expression for a charging case of the load capacitance can be obtained by exchanging *N* and *P* suffixes.

This formula, however, suffers from the above-mentioned problem that the P_S diverges to infinity when C_{OUT}=0. On the other hand, P_S expression for C_{OUT}=0 case, which means that the input rump is slower than the output transition, has been obtained ($P_S(t_T \gg \tau_N)$) as follows [4]

$$P_S(t_T >> \tau_N) = V_{DD} t_T I_{D0P} \frac{1}{\alpha_P + 1} \frac{1}{2^{\alpha_P}} \frac{(1 - v_{TN} - v_{TP})^{\alpha_P + 1}}{(1 - v_{TP})^{\alpha_P}} \quad (3)$$

.

Now, Eq.(1) and Eq.(3) are combined by taking a harmonic average of the two quantities to build the general formula, P_S, which covers both of the slow and fast input case. The resultant expression for P_S is free from the above-mentioned divergence problem.

$$P_S = \frac{1}{\frac{1}{P_S(t_T << \tau_N)} + \frac{1}{P_S(t_T >> \tau_N)}} . \quad (4)$$

This formula expresses the P_S in terms of t_T and can be used to estimate the short-circuit power when input transition time is given. In discussing the scaling characteristics of the short-circuit power dissipation, however, it is better to eliminate t_T by replacing t_T with a function of the saturated drain current of the previous gate stage, I_{D0IN}, and the input node capacitance, C_{IN} [4].

Since the input voltage is the output voltage of another CMOS logic gate, the transient time, t_T, can be expressed as below [4].

$$t_T = \frac{C_{IN} V_{DD}}{I_{D0PIN}} \left(\frac{0.9}{0.8} + \frac{v_{D0P}}{0.8} \ln \frac{10 v_{D0P}}{e} \right) \left(= \frac{C_{IN} V_{DD}}{I_{D0PIN}} k(v_{D0P}) \right) \quad (5)$$

Substituting Eq.(5) into Eq.(4), the short-circuit power dissipation without using t_T is readily obtained as follows.

$$P_S = \frac{k(v_{D0P}) {V_{DD}}^2 C_{IN} fo_P^2}{\frac{v_{D0P} g(v_T, \alpha)}{2k(v_{D0P})} FO \cdot \beta_r + h(v_T, \alpha) fo_P^2} \quad (6)$$

$$k(v_{D0P}) = \frac{0.9}{0.8} + \frac{v_{D0P}}{0.8} \ln \frac{10 v_{D0P}}{e} \quad (7)$$

$$g(v_T, \alpha) = \frac{\alpha_N + 1}{f(\alpha)} \frac{(1 - v_{TN})^{\alpha_N} (1 - v_{TP})^{\alpha_P / 2}}{(1 - v_{TN} - v_{TP})^{\alpha_P / 2 + \alpha_N + 2}} \quad (8)$$

$$h(v_T, \alpha) = 2^{\alpha_P} (\alpha_P + 1) \frac{(1 - v_{TP})^{\alpha_P}}{(1 - v_{TN} - v_{TP})^{\alpha_P + 1}} \quad (9)$$

$$FO = \frac{C_{OUT}}{C_{IN}}, \quad fo_P = \frac{I_{D0P}}{I_{D0PIN}}, \quad \beta_r = \frac{I_{D0P}}{I_{D0N}} \quad (10)$$

III. Comparison between Calculated and SPICE Simulation Results

The calculation results by the proposed formula (Eq.6) agrees well with the SPICE simulation results as shown in Fig.2. Two completely different MOS model parameter sets are used to show the validity of the formula. A CMOS inverter chain shown in Fig.1 is used for the comparison. In Fig. 3, the SPICE simulation results for the dependence of P_S on *FO*(fanout) are compared with the calculation results by the present formula (Eq.6) and the previously published Vemuru et al's formula in Ref.3. Vemuru et al's formula deviates from the simulation results when the fanout is very small and when the fanout is greater than 3. On the other hand, the proposed formula reproduces the simulation results well. The dependence of P_S on I_{D0N}, I_{DOP} and α is also compared between SPICE simulation and the present expression. Figure 4 shows the short-circuit power dependence on PMOS and NMOS drivability ratio, β_r

Again the present formula reproduces the simulation results well. Figure 5 shows the dependence on the MOSFET channel length, L_N and L_P. Since α is changed when the channel length is changed, Fig.5 indicates the validity of the short-circuit power dependence on α_N and α_P of the current formula.

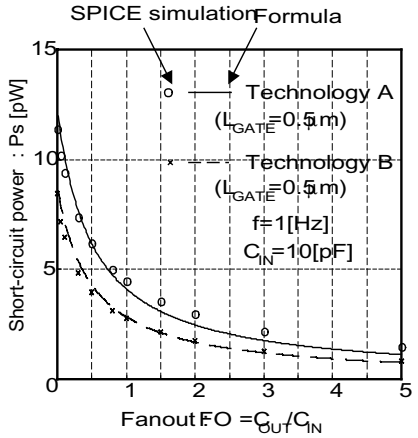

Fig.2 Short-circuit power dependence on fanout(*FO*)

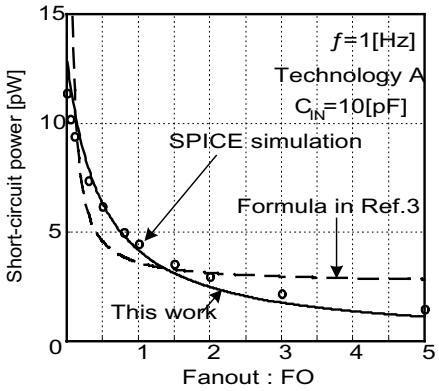

Fig.3 Comparison between this work and Venumu's formula[3]

IV. The Change of The Short-circuit Power Dissipation with Scaling

Now, let us consider the power ratio, $\eta_P = P_S / (P_D + P_S)$, to investigate the impact of the short-circuit power. Using Eq.6, it is straightforward to obtain the power ratio η_P knowing that P_D is expressed as $C_{OUT}V_{DD}^2$. Figure 6 and 7 show comparisons of η_P between calculation and simulation. The dependence of η_P on the threshold voltage and the supply voltage is well reproduced over a wide range of V_{TH} and V_{DD} by the present formula. It is seen from the figures that $P_S / (P_D + P_S)$ is about 10% for a typical design. This means that the contribution of the short-circuit power to the total active power is about 10%.

Can η_P be changed over time? η_P is a function of α, fanout, V_{TH}/V_{DD} and I_{D0}/I_{D0IN} as shown in the following formula

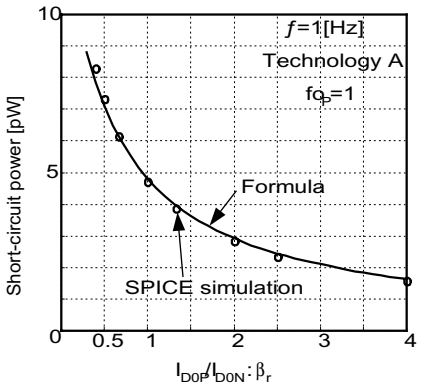

Fig.4 Short-circuit power dependence on β_r

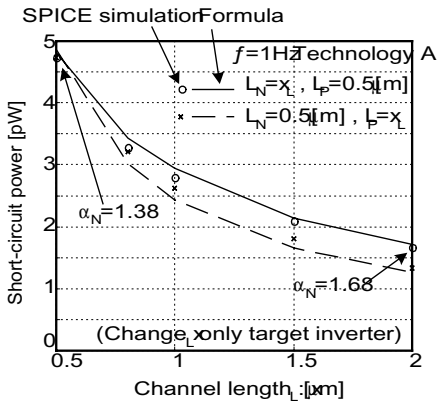

Fig.5 Short-circuit power dependence on channel length

$$\eta_P = \frac{P_S}{P_D + P_S} = \frac{1}{\dfrac{v_{D0P}\, g(v_T,\alpha)}{4k^2(v_{D0P})}\left(\dfrac{FO}{fo}\right)^2 \beta_r + \dfrac{h(v_T,\alpha)}{2k(v_{D0P})}\dfrac{FO}{fo} + 1}. \quad (11)$$

The fanout and I_{D0}/I_{D0IN} are essentially unchanged if the design style is unchanged even if the device is shrunk. α is not a strong function of a device scaling (see Fig.8). Considering the tendency that V_{TH}/V_{DD} will be slightly increasing to keep the standby power in a tolerant level when the supply voltage is decreased as device miniaturization proceeds, the importance of the short-circuit power will not be increased.

V. Conclusions

A simple and closed-form formula for the short-circuit

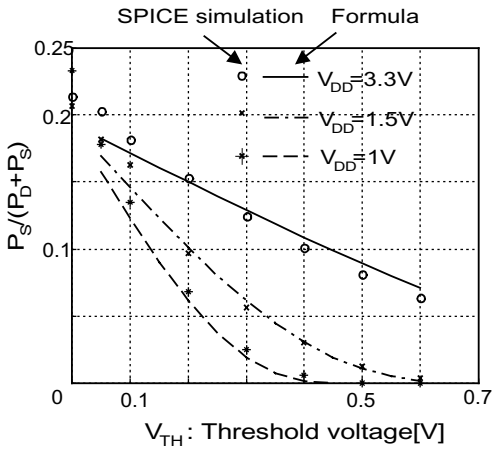

Fig.6 Power ratio dependence on threshold voltage

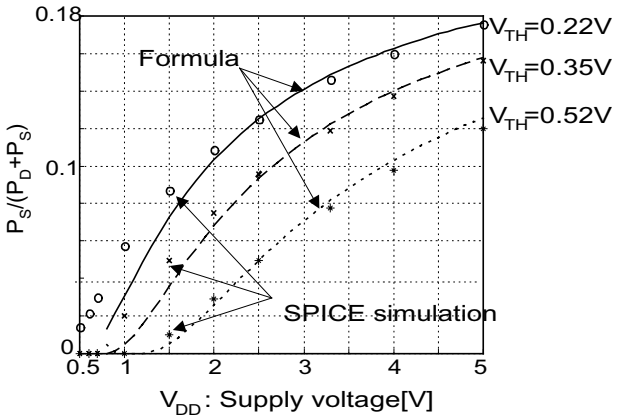

Fig.7 Power ratio dependence on supply voltage

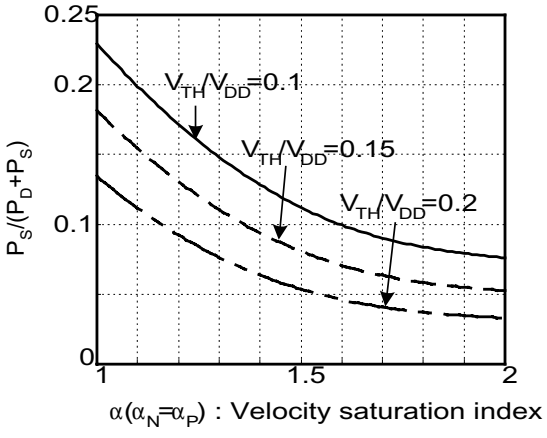

Fig.8 Power ratio dependence on velocity saturation index

power dissipation is derived which correctly reproduces the dependence on various parameters such as a threshold voltage, a supply voltage, a beta ratio, transition time of input voltage, load capacitance and input capacitance. The formula includes the short-channel effects through a velocity saturation index (α) of the α-power law MOSFET model. The formula can be used to estimate the short-circuit power dissipation with more accuracy than the previously published formulas.

By rewriting the formula using fanout and by eliminating the transition time of the input voltage, the scaling characteristics of the short-circuit power is discussed. If the ratio of V_{TH}/V_{DD} is constant, the ratio of the short-circuit power vs. the dynamic power will remain constant even though the V_{DD} is scaled.

It is shown that the short-circuit power monotonically increases as α decreases, as fanout decreases and as the ratio of the threshold voltage over V_{DD} decreases. In order to design low-power, high-speed CMOS VLSI's, a low threshold voltage is sometimes used to achieve sufficient drivability in a low V_{DD} regime. In this case, the effect of the short-circuit power dissipation will increase and become an important part (up to 20%) of the total power dissipation of CMOS VLSI's.

Acknowledgement

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