

# Variable Supply-Voltage Scheme for Low-Power High-Speed CMOS Digital Design

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**Abstract**—This paper describes a variable supply-voltage (VS) scheme. From an external supply, the VS scheme automatically generates minimum internal supply voltages by feedback control of a buck converter, a speed detector, and a timing controller so that they meet the demand on its operation frequency. A 32-b RISC core processor is developed in a 0.4- $\mu\text{m}$  CMOS technology which optimally controls the internal supply voltages with the VS scheme and the threshold voltages through substrate bias control. Performance in MIPS/W is improved by a factor of more than two compared with its conventional CMOS design.

**Index Terms**—Buck converter, low power CMOS circuits, low threshold voltage, low voltage.

## I. INTRODUCTION

LOWERING both the supply voltage  $V_{DD}$  and threshold voltage  $V_{TH}$  enables high-speed, low-power operation [1]–[4]. Fig. 1 depicts equispeed lines (broken lines) and equipower lines (solid lines) on a  $V_{DD}$ - $V_{TH}$  plane calculated from their theoretical models [5], [6]. Typically, circuits are designed at  $V_{DD} = 3.3 \text{ V} \pm 10\%$  and  $V_{TH} = 0.55 \text{ V} \pm 0.1 \text{ V}$  as shown by a rectangle in Fig. 1. This rectangle is a design window because all the circuit specifications should be satisfied within the rectangle for yield-conscious design. In the design window, circuit speed becomes the slowest at the corner *A* while at the corner *B* power dissipation becomes the highest. Therefore, better tradeoffs between speed and power can be found by reducing fluctuations of  $V_{DD}$  and  $V_{TH}$  especially in low  $V_{DD}$  [7], [8]. The equispeed lines and the equipower lines are normalized at the corner *A* and *B* as designated by normalized factor  $\kappa_s$  and  $\kappa_p$ , respectively, so that it can be figured out how much speed and power dissipation are improved or degraded compared to the typical condition by sliding and sizing the design window on the  $V_{DD}$ - $V_{TH}$  plane. For example, at  $V_{DD} = 2.1 \text{ V} \pm 5\%$  and  $V_{TH} = 0.18 \text{ V} \pm 0.05 \text{ V}$  power dissipation can be reduced to about 40% while maintaining the circuit speed. In this way, optimizing  $V_{DD}$  and  $V_{TH}$  is essential in low-power high-speed CMOS design

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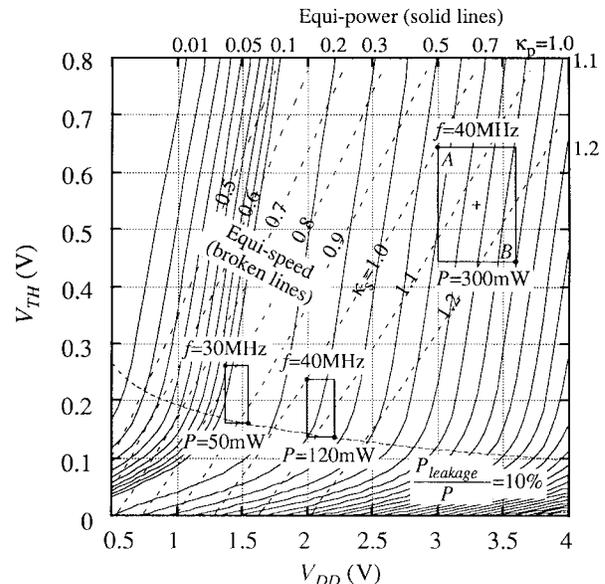


Fig. 1. Exploring low- $V_{DD}$ , low- $V_{TH}$  design space.

while they are given as constant and common parameters in the conventional CMOS design.

$V_{TH}$  can be controlled through substrate bias. A variable threshold-voltage CMOS (VTCMOS) technology is developed [6], [8]–[12]. It dynamically varies  $V_{TH}$  through substrate-bias  $V_{BB}$ .  $V_{BB}$  is controlled so as to compensate  $V_{TH}$  fluctuations in an active mode, while in a standby mode and in the  $I_{DDQ}$  testing, deep  $V_{BB}$  is applied to increase  $V_{TH}$  and cut off subthreshold leakage current. It is reported in [9] that  $V_{TH}$  fluctuations can be reduced to  $\pm 0.05 \text{ V}$  under  $\pm 0.15 \text{ V}$  process fluctuations.

A self-adjusting voltage reduction circuit has been developed [13] using a phase locked loop. However, there has been no report on a digital control scheme. This paper presents a digital circuit scheme to control  $V_{DD}$  on a chip, namely the variable supply-voltage scheme (VS scheme). In the VS scheme, a dc-dc converter [14] generates an internal supply voltage  $V_{DDL}$  very efficiently from an external power supply.  $V_{DDL}$  is controlled by monitoring propagation delay of a critical path in a chip such that it is set to the minimum of voltages in which the chip can operate at a given clock frequency  $f_{ext}$ . This control also reduces  $V_{DDL}$  fluctuations, which is essential in low-voltage design. A 32-b RISC core processor is designed with the VS scheme in the VTCMOS

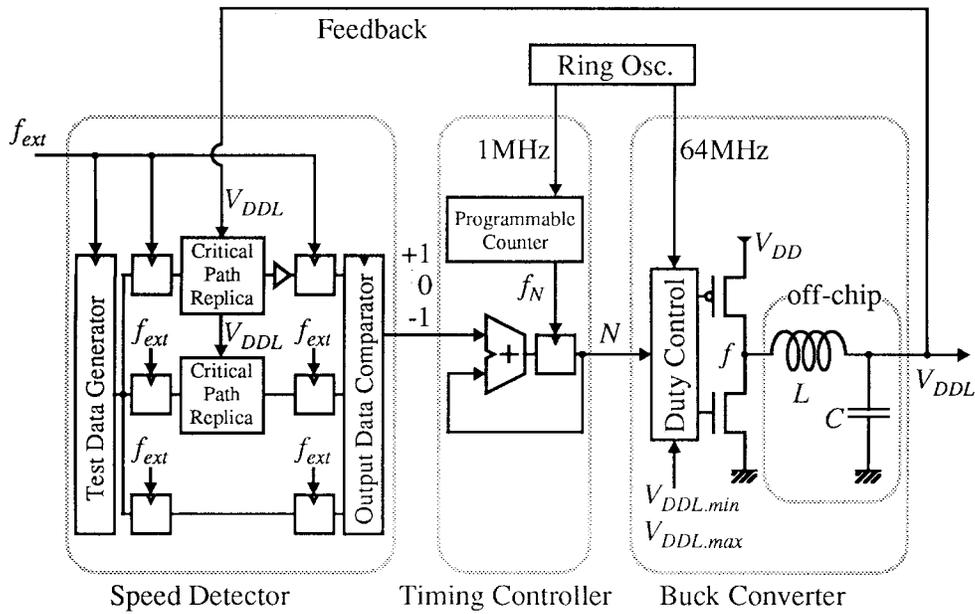


Fig. 2. Variable supply-voltage (VS) scheme.

[15] and achieves more than double the MIPS/W performance compared with the previous CMOS design [16] in the same technology.

In Section II, the VS scheme is described. Circuit implementations are presented in Section III together with a discussion of low-power circuit design. The RISC core with the VS scheme is fabricated in a  $0.4\text{-}\mu\text{m}$  CMOS technology and compared with the previous design. The experimental results are reported in Section IV. Section V is dedicated to conclusions.

## II. VARIABLE SUPPLY-VOLATAGE (VS) SCHEME

The VS scheme is illustrated in Fig. 2. It consists of three parts: 1) a buck converter, 2) a timing controller, and 3) a speed detector. The buck converter generates  $(N/64) \cdot V_{DD}$  for the internal supply voltage  $V_{DDL}$ .  $N$  is an integer from 0 to 63 which is provided from the timing controller. Therefore, the resolution of  $V_{DDL}$  is about 50 mV for  $V_{DD} = 3.3$  V. A duty control circuit generates rectangular waveforms with duty cycle of  $N/64$  whose average voltage is produced by the second-order low-pass filter configured by external inductance  $L$  and capacitance  $C$ . The lower limit of  $V_{DDL}$  can be set in the duty control circuit to assure the minimum operating voltage of a chip. The upper limit can also be set to prevent  $N$  from transiting spuriously from 63 to 0 as a result of noise.

The timing controller calculates  $N$  by accumulating numbers provided from the speed detector, +1 to raise  $V_{DDL}$  and -1 to lower  $V_{DDL}$ . The accumulation is carried out by a clock whose frequency is controlled by a 10-b programmable counter.

The speed detector monitors critical path delay in the chip by its replicas under  $V_{DDL}$ . When  $V_{DDL}$  is too low for the circuit operation in  $f_{ext}$ , the speed detector outputs +1 to raise  $V_{DDL}$ . On the other hand, when  $V_{DDL}$  is too high, the speed detector outputs -1 to lower  $V_{DDL}$ . By this feedback control,

the VS scheme can automatically generate the minimum  $V_{DDL}$  which meets the demand on its operation frequency. For fail-safe control, a small delay is added to the critical path replicas.

Since the speed detection cycle based on  $f_{ext}$  (e.g., 25 ns) is much faster than the time constant of the low-pass filter (e.g.,  $16\ \mu\text{s}$ ) the feedback control may fall into oscillation. The programmable counter in the timing controller adjusts the accumulation frequency  $f_N$  to assure fast and stable response of the feedback control.

There is no interference between the VS scheme and the VTCMOS. The VTCMOS controls  $V_{TH}$  by referring to leakage current of a chip, while the VS scheme controls  $V_{DDL}$  by referring to  $f_{ext}$ .  $V_{DDL}$  is also affected by  $V_{TH}$  because circuit speed is dependent on  $V_{TH}$ . Therefore,  $V_{TH}$  is determined by the VTCMOS, and under the condition,  $V_{DDL}$  is determined by the VS scheme. Since VTCMOS is immune to  $V_{DDL}$  noise [6], there is no feedback from the VS scheme to the VTCMOS, resulting in no oscillation problem between them.

## III. CIRCUIT IMPLEMENTATIONS

### A. Buck Converter

Fig. 3 depicts a circuit schematic of the buck converter. When the output of a 6-b counter  $n$  is between 0 and  $N$ , a pMOS of an output inverter is turned on. When  $n$  is between  $N+1$  and 63, an nMOS of the output inverter is turned on. When  $n$  is between  $N$  and  $N+1$ , and between 63 and 0, neither the pMOS nor the nMOS is turned on to prevent short current from flowing in the large output inverter. The output voltage of the buck converter  $V_{DDL}$  is therefore controlled with 64-step resolution. This resolution causes +50 mV error at  $V_{DDL}$  from  $V_{DD} = 3.3$  V, which yields +3.3%  $V_{DDL}$  error at  $V_{DDL} = 1.5$  V. Note that the error is always positive because the speed detector cannot accept lower  $V_{DDL}$  than a target voltage.

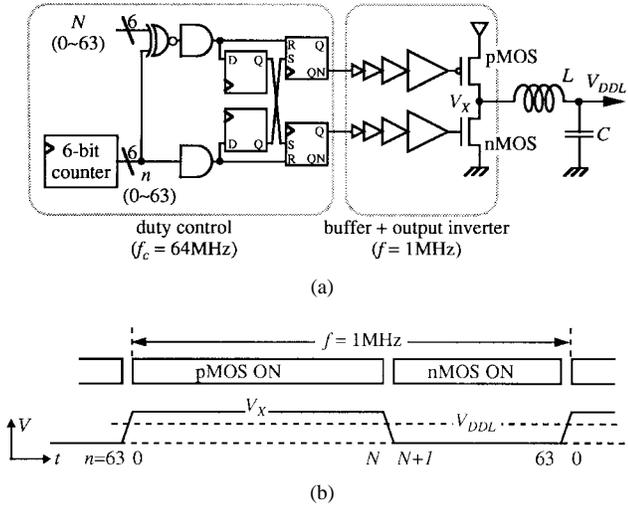


Fig. 3. Buck converter: (a) circuit schematic and (b) timing chart.

The external low-pass filter  $L$  and  $C$ , an effective resistance of the output inverter  $R$ , and its switching period  $\Delta T$  (or switching frequency  $f$ ) should be designed considering dc conversion efficiency  $\eta$ , output voltage ripple when output current is constant  $\Delta V_{out}/V_{out}$ , output voltage drop when output current changes  $\delta V_{out}/V_{out}$ , time constant of the filter as an index of the response  $T_0$ , and pattern area  $S$ .

The efficiency  $\eta$  can be expressed as follows:

$$\eta = \frac{V_{out} I_{out}}{V_{out} I_{out} + I_{out}^2 R + P_{VX} + P_{control}} \quad (1)$$

where  $P_{VX}$  is power dissipation at the output inverter caused by overshoot and undershoot at  $V_X$  from  $V_{DD}$  and ground potential due to inductance current, and  $P_{control}$  is power dissipation of control circuits. Fig. 4 shows simulated waveforms at  $V_X$ . As shown in the figure, inappropriate  $L$  increases  $P_{VX}$ . Its analytical model can be derived from an equivalent  $LCR$  circuit in Fig. 5 with the following two assumptions.

- 1) Duty ratio  $D$  is assumed to be 0.5 for calculation simplicity.
- 2) Damping factor of the low-pass filter is assumed to be one for fast and stable response

$$\xi = \frac{R}{2} \sqrt{\frac{C}{L}} = 1. \quad (2)$$

After the conventional manipulation of differential equations of the equivalent circuit,  $P_{VX}$  is given as follows (see Appendix A for the detailed derivation):

$$P_{VX} \approx \frac{V_{DD}^2}{R} \cdot \frac{\beta^2}{24} \quad (3)$$

where

$$\beta \equiv \frac{\Delta T}{T_0}. \quad (4)$$

$T_0$  is the time constant of the filter which is related to settling time and given by

$$T_0 = \sqrt{LC}. \quad (5)$$

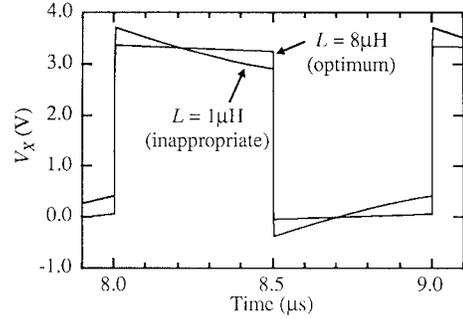


Fig. 4. Simulated waveforms at  $V_X$ .

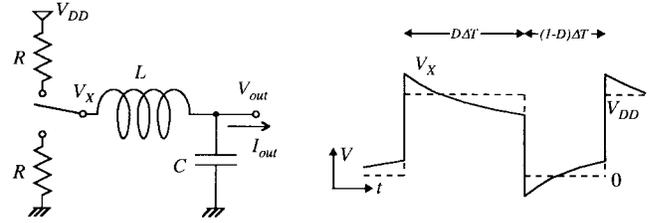


Fig. 5. Equivalent  $LCR$  circuit.

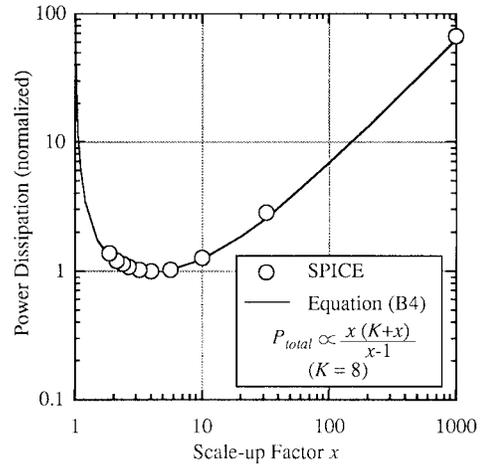


Fig. 6. Power dissipation dependence on scale-up factor in cascaded inverters.

The output voltage ripple when the output current is constant,  $\Delta V_{out}/V_{out}$ , can also be derived from the differential equations and expressed as follows (see Appendix A for the detailed derivation):

$$\frac{\Delta V_{out}}{V_{out}} \approx \frac{\beta^2}{16}. \quad (6)$$

Sudden change in output current causes the output voltage drop  $\delta V_{out}$ . Suppose all the circuits under  $V_{out}$  start to operate at once. The output current changes from zero to  $I_{out}$ . As a result, the filter  $C$  discharges, and  $V_{out}$  drops. Current is then supplied through the filter  $L$  to recover the voltage drop. This recovery time is considered to be an order of  $T_0$ . So the amount of charge of  $I_{out} \cdot T_0$  is derived from  $C$  to yield the voltage drop of  $I_{out} \cdot T_0/C$ . The output voltage drop when the output current changes  $\delta V_{out}/V_{out}$  is therefore approximately

given by

$$\frac{\delta V_{\text{out}}}{V_{\text{out}}} \approx \frac{I_{\text{out}} \cdot T_0}{C \cdot V_{\text{out}}}, \quad (7)$$

$P_{\text{control}}$ , on the other hand, is written as

$$P_{\text{control}} = \alpha_c N_{\text{max}} f C_c V_{\text{DD}}^2 + f C_{\text{buffer}} V_{\text{DD}}^2 + \alpha_{\text{replica}} f_{\text{ext}} C_{\text{replica}} V_{\text{out}}^2 \quad (8)$$

where

$$f = \frac{1}{\Delta T}. \quad (9)$$

The first term is power dissipation of the duty control circuits where operating frequency is  $N_{\text{max}} \cdot f$ .  $N_{\text{max}}$  is the output voltage resolution which is 64 in this design. The second term is power dissipation of the buffer circuit in the buck converter, and the third term is power dissipation of the replica circuits in the speed detector. In each term,  $\alpha$  is switching probability and  $C$  is capacitance.

Since most of the layout pattern is occupied by the large inverter and the buffer circuits, pattern area can be expressed as

$$S = \frac{S_1}{R} + S_2 \quad (10)$$

where  $S_1$  and  $S_2$  are constants.

From these equations, the smaller  $\beta$  is, the smaller  $P_{\text{VX}}$  is and the smaller the output voltage ripple. On the other hand, for the smaller settling time, the smaller  $T_0$  is preferable. Therefore,  $\Delta T$  should be reduced, which in turn increases  $P_{\text{control}}$ . In this way there are tradeoffs among these parameters.

For example, under the following constraints:

- Output voltage:  $V_{\text{out}} = 2.1 \text{ V}$ ;
- Output current:  $I_{\text{out}} = 67 \text{ mA}$  ( $P_{\text{out}} = 140 \text{ mW}$ );
- Output voltage ripple when output current is constant:  $\Delta V_{\text{out}}/V_{\text{out}} < 0.1\%$ ;
- Output voltage drop when output current changes:  $\delta V_{\text{out}}/V_{\text{out}} < 2\%$ ;
- Filter time constant (related to settling time):  $T_0 < 100 \mu\text{s}$ ;
- Pattern area:  $S < 500 \mu\text{m}^2$ ;
- dc-dc efficiency:  $\eta = \text{maximum}$ .

$L$ ,  $C$ ,  $R$ , and  $f$  can be numerically solved as follows.

- Low-pass filter inductance:  $L = 8 \mu\text{H}$ ;
- Low-pass filter capacitance:  $C = 32 \mu\text{F}$ ;
- Output inverter effective resistance:  $R = 1 \Omega$ ;
- Output inverter switching frequency:  $f = 1 \text{ MHz}$ .

For the equivalent  $R = 1 \Omega$  in the output inverter, transistor size of the pMOS and the nMOS is as large as 7.6 mm and 3.8 mm, respectively. Cascaded inverters are necessary to drive the output inverter with a typical inverter whose pMOS and nMOS transistor size is about 8  $\mu\text{m}$  and 4  $\mu\text{m}$ , respectively. When transistor size ratio of the final stage ( $W_n$ ) to the first stage ( $W_0$ ) of the cascaded inverters is given, the optimum scale-up factor  $x$  and the optimum number of stages  $n$  to minimize the power dissipation are given by (see Appendix B for the

detailed derivation)

$$x = 1 + \sqrt{1 + K} \quad (11)$$

$$n = \frac{\log\left(\frac{W_n}{W_0}\right)}{\log x} \quad (12)$$

where  $K$  is the ratio of power dissipation due to capacitance charging and discharging to power dissipation due to crowbar current when  $x = 1$ . From simulation study depicted in Fig. 6, the above equations hold very accurately with  $K = 8$ . The optimum scale-up factor  $x$  becomes four, and the optimum number of stages,  $n$  becomes five in this design.

### B. Speed Detector

A circuit schematic of the speed detector is shown in Fig. 7(a). It has three paths under  $V_{\text{DDL}}$ : 1) a critical path replica of the chip ‘‘CPR,’’ 2) the same critical path replica with inverter gates equivalent to 3% additional delay ‘‘CPR+,’’ and 3) direct connection between flip-flops ‘‘REF.’’ Since the direct connection can always transmit the test data correctly within the cycle time of  $f_{\text{ext}}$  even in low  $V_{\text{DDL}}$ , it can be referred to as a correct data. Other paths may output wrong data when the delay time becomes longer than the cycle time of the given  $f_{\text{ext}}$  at the given  $V_{\text{DDL}}$ . By comparing the outputs of these paths with that of the direct connection, it can be deduced whether or not the chip operates correctly in  $f_{\text{ext}}$  at  $V_{\text{DDL}}$ . When  $V_{\text{DDL}}$  is not high enough, the outputs of the two paths ‘‘CPR’’ and ‘‘CPR+’’ are both wrong, and the speed detector outputs +1 to raise  $V_{\text{DDL}}$ . When  $V_{\text{DDL}}$  is higher, equivalent to more than 3% delay in the critical path than the given  $f_{\text{ext}}$ , the outputs of the two paths are both correct, and the speed detector outputs  $-1$  to lower  $V_{\text{DDL}}$ . When  $V_{\text{DDL}}$  is in between, the output of the critical path ‘‘CPR’’ is correct and that of the longer path ‘‘CPR+’’ is wrong, and the speed detector outputs 0 to maintain  $V_{\text{DDL}}$ . This nondetecting voltage gap is necessary to stabilize  $V_{\text{DDL}}$  but yields an offset error. The offset error should be minimized but no smaller than the minimum resolution of the  $V_{\text{DDL}}$ . This is because if the gap is smaller than the resolution, no  $V_{\text{DDL}}$  level may exist in the voltage gap. This may cause the output voltage ripple as large as the resolution. The 3% additional delay corresponds to 80 mV in  $V_{\text{DDL}}$ , which is larger than the resolution of 50 mV. In total,  $V_{\text{DDL}}$  may have 130 mV offset error.

A timing chart of the speed detector is illustrated in Fig. 7(b). The test data in this figure is an example of the critical path becoming critical in propagating a low-to-high signal. The test is performed every eight clock cycles. The other seven clock cycles are necessary in low  $V_{\text{DDL}}$  for not evaluating test data provided before.  $V_{\text{DDL}}$  can be set at very low voltages where the propagation delay becomes eight multiples of the cycle time of  $f_{\text{ext}}$ . This mislocking, however, can be avoided by setting the lower limit of  $V_{\text{DDL}}$  in the timing controller. The compared results are registered by flip-flops which are held by a hold signal as shown in Fig. 7(a) until the next evaluation.

Since the critical path replicas operate at  $V_{\text{DDL}}$ , the signals need to be level-shifted to  $V_{\text{DD}}$ . A sense-amplifier flip-flop [17] is employed to perform level-shifting and registering simultaneously.

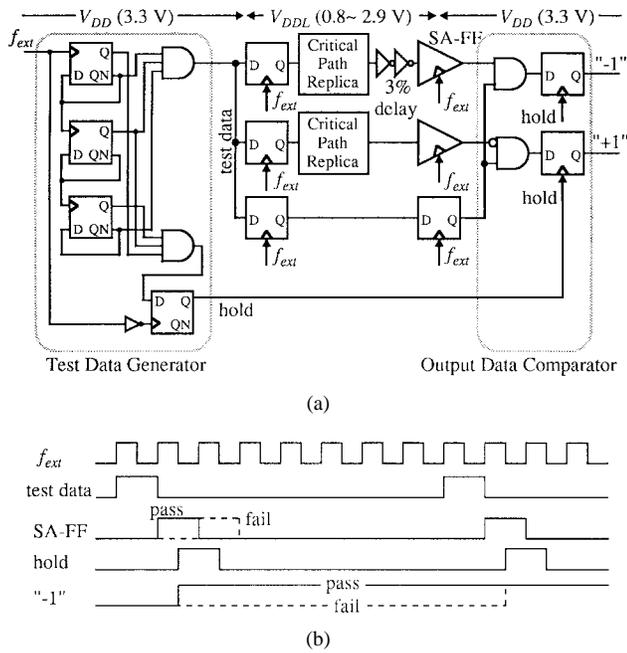


Fig. 7. Speed detector: (a) circuit schematic and (b) timing chart.

### C. Timing Controller

A timing controller adjusts the control frequency of  $N$ ,  $f_N$ , to realize fast and stable response of the feedback control. The higher the  $f_N$ , the faster the response but the lower the stability. Conventional stability analysis and compensation techniques, however, are rather difficult to apply for several reasons. In the speed detector, circuit speed is a nonlinear function of  $V_{DDL}$ . Its output is +1 or -1 regardless of the magnitude of the error in  $V_{DDL}$ . Most of the control is performed in digital while the low-pass filter is analog. With these difficulties, a programmable counter is introduced as a practical way to control  $f_N$ . Based upon experimental evaluation, the optimum  $f_N$  can be found and set to the programmable counter.

Fig. 8 depicts simulation results of  $V_{DDL}$  after power-on. When  $f_N$  is 1 MHz, much faster than the roll-off frequency of the low-pass filter, 10 kHz, oscillation appears in  $V_{DDL}$ . When  $f_N$  is 62.5 kHz, on the other hand, the response of  $V_{DDL}$  is fast and stable.  $V_{DDL}$  can reach the target voltage in 100  $\mu$ s after power-on.

## IV. EXPERIMENTAL RESULTS

A 32-b RISC core processor R3900 is implemented by about 440 k transistors, including a 32-b multiply/accumulate (MAC) unit, a 4-kB direct mapped instruction cache, and a 1-kB two-way set-associative data cache [16]. Layout is slightly modified for the VS scheme and the VTCMOS. A VS macro and a VT macro are added at the corners of the chip. Many of the substrate contacts are removed [12] and the rest are connected to the VT macro. The chip is fabricated in a 0.4- $\mu$ m CMOS n-well/p-sub double-metal technology. A chip micrograph appears in Fig. 9. Main features are summarized in Table I. The VS and the VT macros occupies  $0.45 \times 0.59 \text{ mm}^2$

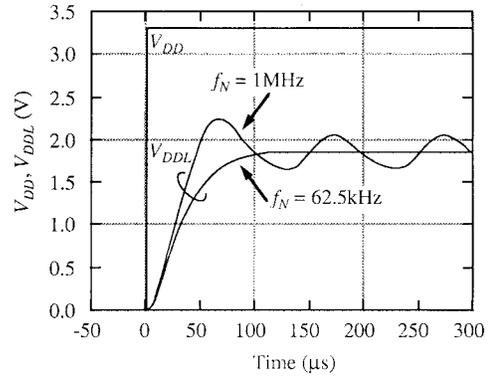


Fig. 8. Simulated  $V_{DDL}$  response after power-on.

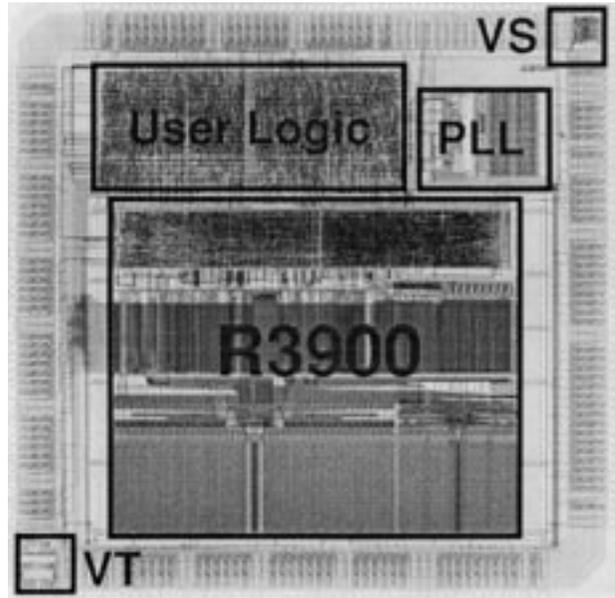


Fig. 9. Chip micrograph.

TABLE I  
FEATURES

Technology	0.4 $\mu$ m CMOS, n-well/p-sub, double-metal, $V_{TH} = 0.05 \text{ V} \pm 0.1 \text{ V}$
Compensated $V_{TH}$	$0.2 \text{ V} \pm 0.05 \text{ V}$
External $V_{DD}$	$3.3 \text{ V} \pm 10\%$
Internal $V_{DDL}$	$0.8 \text{ V} \sim 2.9 \text{ V} \pm 5\%$
Power dissipation	140 mW @ 40 MHz
Chip size	$8.0 \times 8.0 \text{ mm}^2$
VS macro size	$0.45 \times 0.59 \text{ mm}^2$
VT macro size	$0.49 \times 0.72 \text{ mm}^2$

and  $0.49 \times 0.72 \text{ mm}^2$ , respectively. The total area penalty of the two macros is less than 1% of the chip size.

Fig. 10 is a shmoo plot of the RISC processor. The RISC core operates at 40 MHz at 1.9 V, and at 10 MHz at 1.3 V. In this figure, measured  $V_{DDL}$  versus  $f_{ext}$  are also plotted. The VS scheme can generate the minimum  $V_{DDL}$  of the voltages where the circuit can operate at  $f_{ext}$ . Practically fail-free operation should be guaranteed. The VS scheme should be designed such that  $V_{DDL}$  is controlled to sit sufficiently inside of the pass region in the shmoo plot by adding supplementary gates to the critical path replicas.

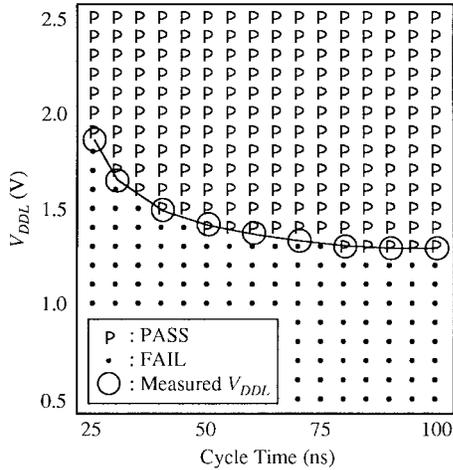


Fig. 10. Shmoo plot of R3900 and measured  $V_{DDL}$ .

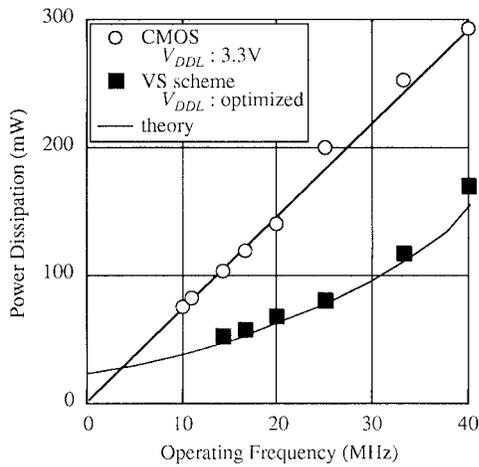


Fig. 11. Measured power dissipation versus operating frequency.

Fig. 11 shows a measured power dissipation of the RISC core without I/O. White circles and black squares in this figure represent power dissipation at 3.3 V and  $V_{DDL}$  determined by the VS scheme, respectively. The VS scheme can reduce power by an amount larger than that which can be achieved by reducing clock frequency. The power dissipation at  $f_{ext} = 0$  in the VS scheme is about 20 mW, which comes from the dc-dc converter. This power loss is mainly due to circuits for experimental purposes and can be reduced to lower than 10 mW. The dc-dc efficiency  $\eta$  is measured and plotted in Fig. 12. The left side of the peak is degraded by the power dissipation in dc-dc itself, while the right side of the peak is degraded by parasitic resistance. Due to the power dissipation of the experimental circuits and due to high contact resistance of about  $6 \Omega$  in a probe card, the maximum efficiency is lower than anticipated. If the experimental circuits are removed and the chip is bond-wired in a package, the maximum efficiency is estimated to be higher than 85%.

Measure performance in MIPS/W are 320 MIPS/W at 33 MHz, and 480 MIPS/W at 20 MHz, which are improved by a factor of more than two compared with that of the previous design, 150 MIPS/W [16].

Fig. 13 shows measured  $V_{DDL}$  voltage regulated by the VS scheme when  $V_{DD}$  is varied by about 50%. The robustness

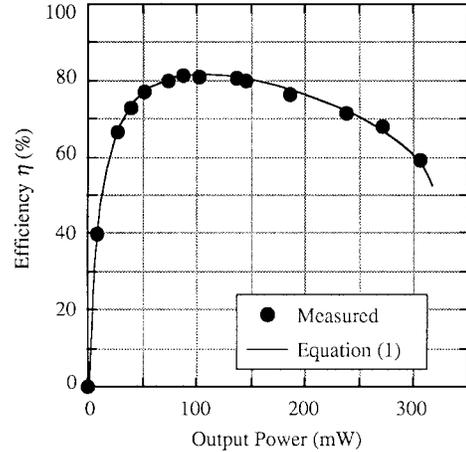


Fig. 12. Measured dc-dc efficiency.

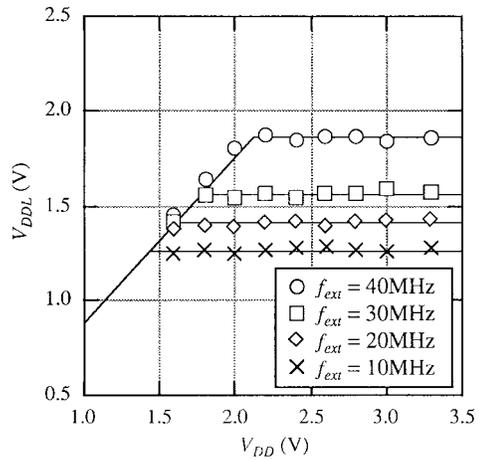


Fig. 13. Measured  $V_{DDL}$  versus  $V_{DD}$ .

to the supply-voltage change is clearly demonstrated.  $V_{DDL}$  is regulated at a target voltage as long as  $V_{DD}$  is higher than the target.

## V. CONCLUSION

The VS scheme is presented and examined. The VS scheme can minimize internal supply voltages automatically according to its operating frequency and reduces voltage fluctuations. The 300 MIPS/W RISC core processor with the VS scheme in the VTCMOS has been fabricated. Performance in MIPS/W has been improved by a factor of more than two compared with the previous design just by adding the VS macro and the VT macro. Area penalty is smaller than 1%.

## APPENDIX A

### DERIVATION OF POWER EQUATIONS FROM EQUIVALENT LCR CIRCUIT

Differential equations of the equivalent circuit in Fig. 5 are given by

$$\left( LC \frac{d^2}{dt^2} + CR \frac{d}{dt} + 1 \right) \cdot V_{out}^{(1)}(t) = V_{DD} \quad (A1)$$

$$I_L^{(1)}(t) = C \frac{dV_{out}^{(1)}}{dt} \quad (A2)$$

when  $0 \leq t \leq D\Delta T$  (pMOS is on), and

$$\left( LC \frac{d^2}{dt^2} + CR \frac{d}{dt} + 1 \right) \cdot V_{\text{out}}^{(2)}(t) = 0 \quad (\text{A3})$$

$$I_L^{(2)}(t) = C \frac{dV_{\text{out}}^{(2)}}{dt} \quad (\text{A4})$$

when  $D\Delta T \leq t \leq \Delta T$  (nMOS is on).

With the following boundary conditions:

$$V_{\text{out}}^{(1)}(t = D\Delta T) = V_{\text{out}}^{(2)}(t = D\Delta T) \quad (\text{A5})$$

$$I_L^{(1)}(t = D\Delta T) = I_L^{(2)}(t = D\Delta T) \quad (\text{A6})$$

$$V_{\text{out}}^{(2)}(t = \Delta T) = V_{\text{out}}^{(1)}(t = 0) \quad (\text{A7})$$

$$I_L^{(2)}(t = \Delta T) = I_L^{(1)}(t = 0) \quad (\text{A8})$$

and the following two assumptions discussed in Section III-A:

$$\xi = \frac{R}{2} \sqrt{\frac{C}{L}} = 1 \quad (\text{A9})$$

$$D = 0.5 \quad (\text{A10})$$

the differential equations can be solved as follows:

$$V_{\text{out}}^{(1)}(t) = V_{\text{DD}} \left\{ 1 - \left( P + Q \cdot \frac{t}{T_0} \right) e^{-\frac{t}{T_0}} \right\} \quad (\text{A11})$$

$$V_{\text{out}}^{(2)}(t) = V_{\text{DD}} \left\{ P + Q \left( \frac{t}{T_0} - \frac{\beta}{2} \right) \right\} e^{-\left( \frac{t}{T_0} - \frac{\beta}{2} \right)} \quad (\text{A12})$$

where

$$P \equiv \frac{\left( 1 - \frac{\beta}{2} \right) e^{-\frac{\beta}{2}} + 1}{\left( 1 + e^{-\frac{\beta}{2}} \right)^2} \quad (\text{A13})$$

$$Q \equiv \frac{1}{1 + e^{-\frac{\beta}{2}}} \quad (\text{A14})$$

$$T_0 \equiv \sqrt{LC} \quad (\text{A15})$$

$$\beta \equiv \frac{\Delta T}{T_0}. \quad (\text{A16})$$

$V_X$  is therefore given by

$$\begin{aligned} V_X^{(1)}(t) &= V_{\text{DD}} - R \cdot I^{(1)}(t) \\ &= V_{\text{DD}} \left[ 1 - 2 \left\{ P - \left( 1 - \frac{t}{T_0} \right) Q \right\} e^{-\frac{t}{T_0}} \right] \end{aligned} \quad (\text{A17})$$

$$\begin{aligned} V_X^{(2)}(t) &= -R \cdot I^{(2)}(t) \\ &= 2V_{\text{DD}} \left[ P - \left\{ 1 - \left( \frac{t}{T_0} - \frac{\beta}{2} \right) \right\} Q \right] e^{-\left( \frac{t}{T_0} - \frac{\beta}{2} \right)}. \end{aligned} \quad (\text{A18})$$

Since  $P_{V_X}$  is power dissipation at the output inverter caused by overshoot and undershoot at  $V_X$  from  $V_{\text{DD}}$  and ground potential, it can be calculated by

$$\begin{aligned} P_{V_X} &= \frac{1}{\Delta T} \cdot \left[ \int_0^{\frac{\Delta T}{2}} \frac{1}{R} \left\{ V_{\text{DD}} - V_X^{(1)}(t) \right\}^2 dt \right. \\ &\quad \left. + \int_{\frac{\Delta T}{2}}^{\Delta T} \frac{1}{R} \left\{ -V_X^{(2)}(t) \right\}^2 dt \right] \\ &= \frac{V_{\text{DD}}^2}{R} \cdot \frac{2}{\beta} \cdot \frac{1 - \beta e^{-\frac{\beta}{2}} - e^{-\beta}}{1 - e^{-\frac{\beta}{2}}} \end{aligned} \quad (\text{A19})$$

$$\approx \frac{V_{\text{DD}}^2}{R} \cdot \frac{\beta^2}{24} \quad (\beta \ll 1). \quad (\text{A20})$$

Since we assume  $D = 0.5$ ,  $V_{\text{out}}$  is  $V_{\text{DD}}/2$ . The maximum output ripple can be expressed by

$$\frac{\Delta V_{\text{out}}}{2} = \left| V_{\text{out}}(t = t_0) - \frac{V_{\text{DD}}}{2} \right| \quad (\text{A21})$$

$$\left. \frac{dV_{\text{out}}}{V_{\text{out}}} \right|_{t=t_0} = 0. \quad (\text{A22})$$

Solving these equations we obtain

$$\frac{\Delta V_{\text{out}}}{V_{\text{out}}} = 2 \left[ \frac{2 \exp \left\{ -\frac{\beta e^{-\frac{\beta}{2}}}{2(1+e^{-\frac{\beta}{2}})} \right\}}{1 + e^{-\frac{\beta}{2}}} - 1 \right] \quad (\text{A23})$$

$$\approx \frac{\beta^2}{16}. \quad (\text{A24})$$

## APPENDIX B

### POWER OPTIMIZATION OF CASCADED INVERTER STAGES

In this appendix, optimum scale-up of a chain of CMOS inverters for minimum power dissipation is discussed when transistor size ratio of the final stage to the first stage is given. This problem can be seen not only in the dc-dc converter but also in an output pad where the output transistor size is given from specifications such as drive capability.

Power dissipation in the  $i$ th stage can be expressed as follows:

$$P_i = P_{c_i} + P_{s_i} \quad (\text{B1})$$

where  $P_{c_i}$  is power dissipation due to charging and discharging and  $P_{s_i}$  is power dissipation due to crowbar current. Let us assume that  $P_{c_i}$  is proportional to transistor width  $W_i$  and that  $P_{s_i}$  is proportional to  $W_i$  and inversely proportional to signal slope. Let us also assume that the signal slope is proportional to  $W_{i-1}/W_i$  because driving current is proportional to  $W_{i-1}$  and loading capacitance is proportional to  $W_i$ . Then  $P_{c_i}$  and  $P_{s_i}$  are given by

$$P_{c_i} = u W_i \quad (\text{B2})$$

$$P_{s_i} = v W_i \cdot \frac{W_i}{W_{i-1}} \quad (\text{B3})$$

where  $u$  and  $v$  are constants. Total power dissipation is therefore given by

$$P_{\text{total}} = \sum P_i = v(M-1) \cdot \frac{x(K+x)}{x-1} \cdot W_0 \quad (\text{B4})$$

where

$$x = \frac{W_i}{W_{i-1}} \quad (\text{for all } i) \quad (\text{B5})$$

$$M = \frac{W_n}{W_0} = x^n \quad (\text{B6})$$

$$K = \frac{u}{v}. \quad (\text{B7})$$

When  $\partial P_{\text{total}}/\partial x = 0$  the total power dissipation becomes minimum. Then

$$x = 1 + \sqrt{1 + K} \quad (\text{B8})$$

$$n = \frac{\log\left(\frac{V_{DD}}{V_0}\right)}{\log x}. \quad (\text{B9})$$

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