FP 12.4: A CMOS Scheme for 0.5V Supply Voltage with Pico-Ampere Standby Current

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Recently, low-power requirements are getting stronger in VLSI designs. Since the power consumption of CMOS VLSIs quadratically depends on the supply voltage, low-voltage circuits have been exploited. If a VLSI is operated in 0.5V~0.8V V_{DD} range for low-power consumption, the threshold voltage of MOSFETs, V_{TH}, should be well below 0.5V to turn the MOSFETs on. V_{TH} between 0.1V and 0.2V causes 10nA-order subthreshold leakage current per logic gate in a standby mode, which leads to 10mA standby current for 1M-gate VLSIs. This hinders application of the VLSIs in mobile equipment powered by a small battery. The super cut-off CMOS (SCCMOS) circuit overcomes this problem. With the SCCMOS, operation is possible below 0.5V~0.8V V_{DD} with 0.1V~0.2V V_{TH} and, at the same time, pA-order standby current per logic gate can be achieved.

Figure 1 shows a circuit diagram of the SCCMOS for a pMOS insertion case. Low-V_{TH} pMOS, M1, whose V_{TH} is 0.1V~0.2V is inserted in series with a low-V_{TH} circuit block. The gate of the inserted pMOS is applied 0V in an active mode and is over driven to ~0.9V in standby. A p-type substrate is widely used and the body of pMOSFETs can be connected to the virtual V_{DD} line, which does not require another line for the pMOS body bias. Therefore, modification to the cell library is not needed. nMOS insertion is possible where the gate of the inserted nMOS is driven to about -0.4V in standby to fully cut off leakage current. The gate bias generator can be without a feedback loop as is shown in the figure because an exact control of the voltage is not needed. Figure 1 shows a technique to reduce the voltage across the gate oxide that can be used when oxide reliability is an issue.

There are other ways to realize speed at low-V_{DD}. Multi-threshold CMOS (MTCMOS) uses high-V_{TH} devices (0.6V~0.7V) in series to low-V_{TH} transistor circuits to fully cut off the leakage current in standby [1]. MTCMOS does not work below 0.7V V_{DD} because the high-V_{TH} MOSFET does not turn on. Variable threshold CMOS (VTCMOS) applies backgate bias to fully cut off the subthreshold current in standby [2, 3]. The scheme can not be applied to fully-depleted SOI devices and is difficult to apply to partially-depleted SOI circuits due to the overhead needed to apply body bias. Another drawback is that the VTCMOS requires modifications to cell libraries to separate substrate/well bias lines from supply voltage lines.

Dynamic threshold MOS (DTMOS) suffers from 10mA-range leakage current at 0.5V~0.7V V_{DD} for 1M-gate VLSIs in standby because of the inherent forward bias current of pn-junctions [4]. SCCMOS in conjunction with DTMOS cuts off the leakage current in standby and retains the speed of the DTMOS in active. VTCMOS can not be used in conjunction with the DTMOS where a backgate is always fixed to a gate voltage.

A test chip fabricated using 0.3µm triple-metal CMOS process with 0.2V V_{TH} demonstrates feasibility of the SCCMOS. A micrograph is shown in Figure 2. Measured speed of an inverter and 2-input NAND gate with fanout of three are shown in Figure 3. MOSFET gate widths in the logic gates are 2.4µm and width of the serially inserted MOSFET is 10µm. The SCCMOS pushes the low-voltage operation limit of CMOS logic over the MTCMOS. Measured leakage is below 1pA per gate in standby.

The gate bias generator is 100x100µm^2 and the power consumption is 0.1µA with 10kHz pumping frequency. Active power consumption of a fanout-3 NAND gate is 8fJ per switching.

When the circuit is in standby, the virtual V_{DD} drops to 0V due to high leakage of the low-V_{TH} circuits. Then flip-flops in the low-V_{TH} circuits lose stored information in standby. One way to solve the problem at a system level is to scan all information stored in flip-flops into a memory before entering standby and to restore the information into flip-flops at resume using scan-path flip-flops. When this does not work, a special flip-flop in Figure 4 can be used. The waveforms are also shown in the figure. The basic current-latch flip-flop is a low-power flip-flop extensively used in design. The flip-flop is made of low-V_{TH} devices for speed with serial cut-off MOSFET and SRAM cell is added to the basic flip-flop.

The SRAM storage element is composed of high-V_{TH} MOSFETs (0.6V) to suppress leakage current in standby. The source voltage of the SRAM cell is -0.5V to obtain strong drive in the resume process. If the drive is low, it can not write the stored information back into the output node of the cross-coupled NORs.

Figure 5 is a measured speed characteristics of the flip-flop. Numbers in the figure signify gate width. To measure flip-flop speed, a flip-flop chain with edge-trigger pulse generators is used and delay of the edge-trigger pulse generators is subtracted to get the flip-flop delay. -0.5V is applied to the p-substrate to prevent pn-junction forward bias. Since the process is not triple-well, -0.5V backgate bias increases the V_{TH} of nMOSs to 0.3V. This is why the flip-flop is slow. With a triple-well technology, flip-flop delay is decreased to three times the inverter delay with fanout of three.

Figure 6 shows a measured speed characteristics of pass-transistor logic (PTL) in SCCMOS. The PTL provides area efficiency. The schematic, also shown in the figure, is single-rail implementation with small feedback pMOS for restoring V_{TH} drop with the series nMOS connection. Operation with 1V V_{DD} is certified.

The PTL test circuit uses a gate-array structure in Figure 7. Cell structure is optimized for single-rail PTL and is simpler than previously published basic cell structure [5]. SRAM cells can also be designed with the basic cell as in Figure 7.

Acknowledgments:

The authors acknowledge Toshiba Corp. for support in preparing the test chip and T. Furuyama, T. Kuroda, T. Fujita, Y. Watanabe, M. Hamada for discussions.

References:

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[2] Seta, K., et al., "50% Active Power Saving without Speed Degradation Using Standby Power Reduction (SPR) Circuit," ISSCC Digest of Technical Papers, pp. 318-319, Feb., 1995.

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[4] Fuse, T., et al., "A 0.5V 200MHz 1-Stage 32b ALU Using a Body Bias Controlled SOI Pass-Gate Logic," ISSCC Digest of Technical Papers, pp. 286-287, Feb., 1997.

[5] Sasaki, Y., et al., "Pass Transistor Based Gate Array Architecture," Symp. on VLSI Circuits Dig. Tech. Papers, pp. 123-124, June, 1995.

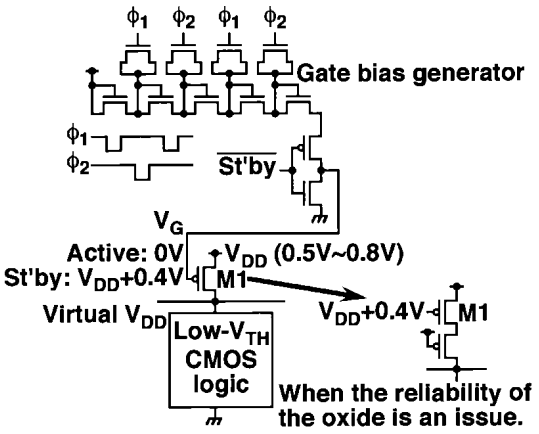

Figure 1: Super cut-off CMOS (SCCMOS) scheme.

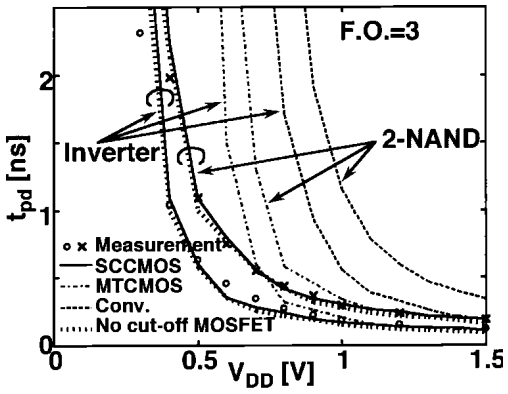

Figure 3: Speed of inverter and NAND with SCCMOS.

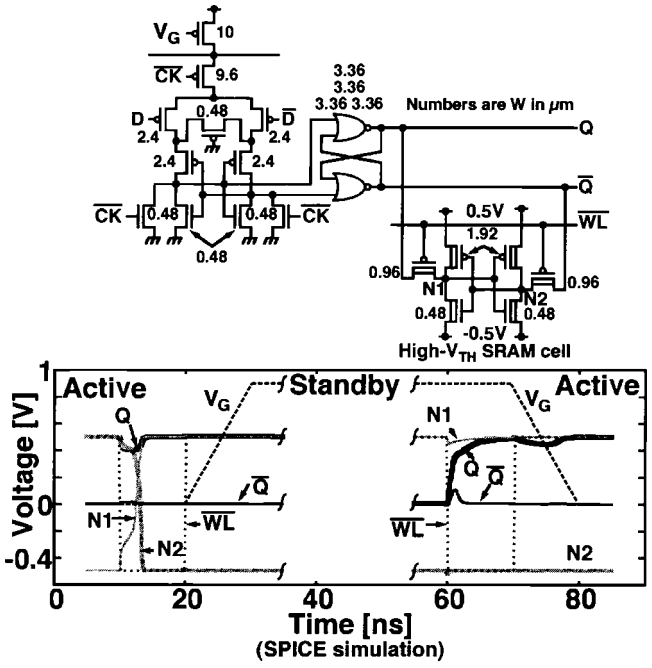

Figure 4: SCCMOS flip-flop and operating waveforms.

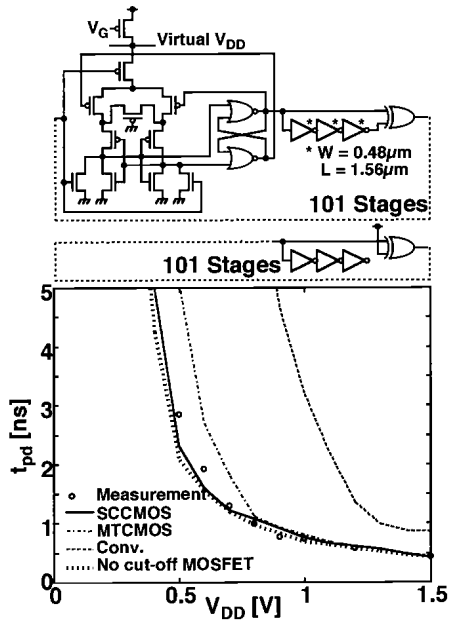

Figure 5: Speed of flip-flop with SCCMOS.

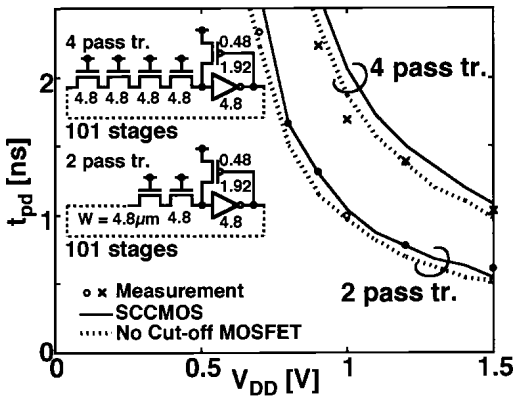

Figure 6: Speed of PTL with SCCMOS.

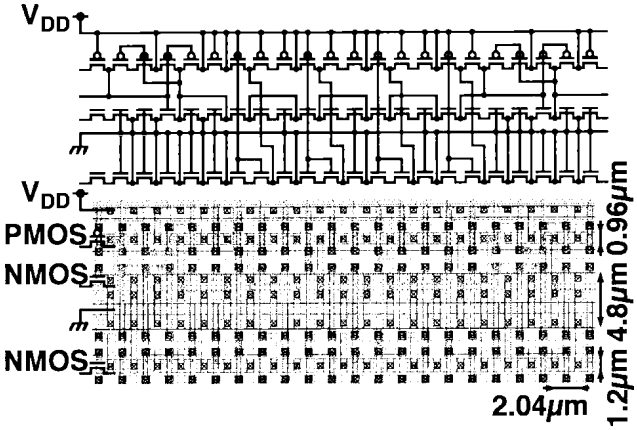

Figure 7: PTL oriented gate array.

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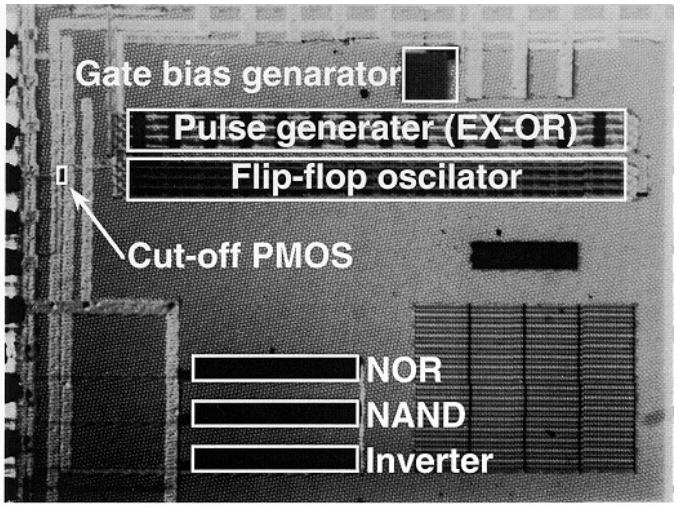
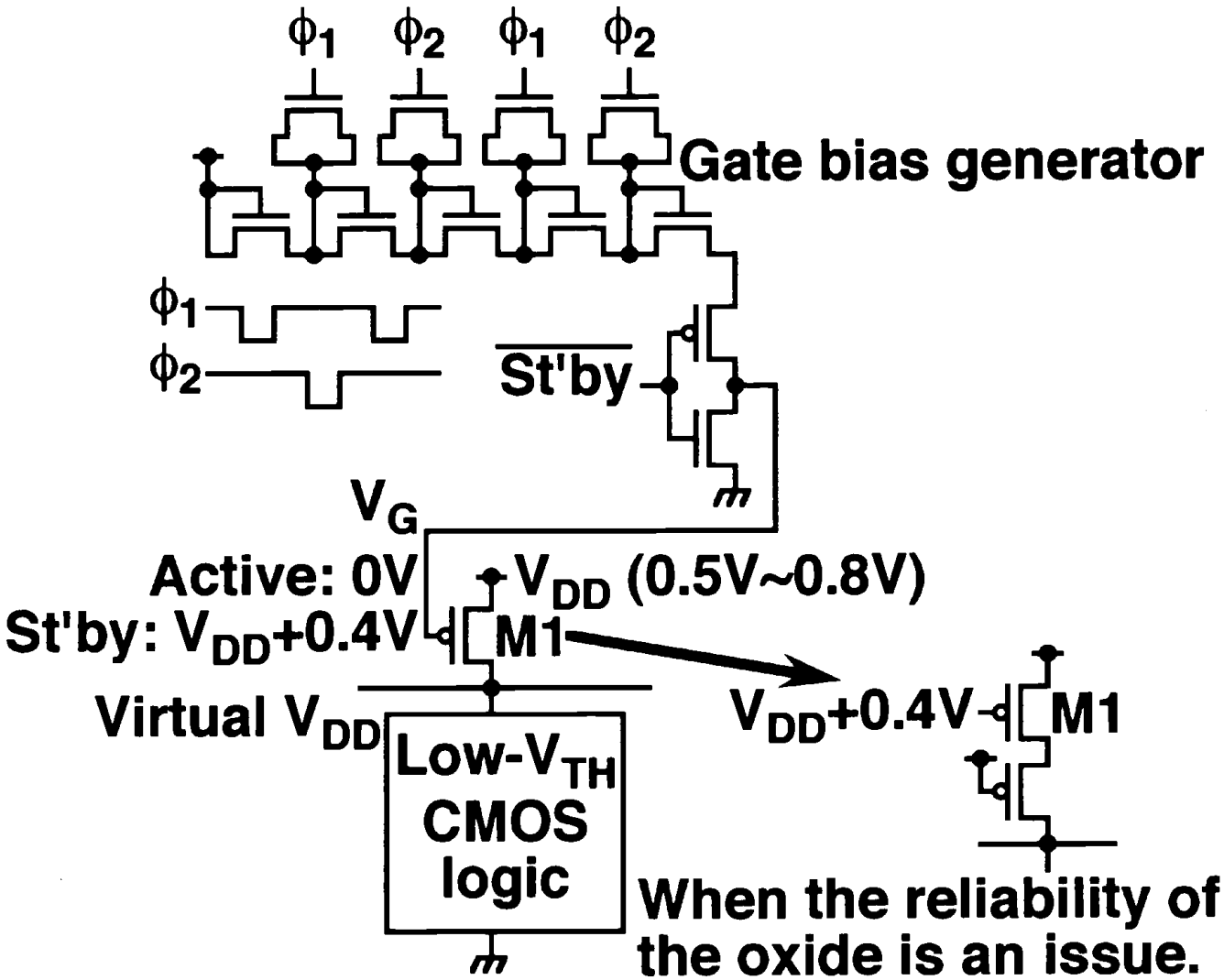


Figure 2: Test chip micrograph.



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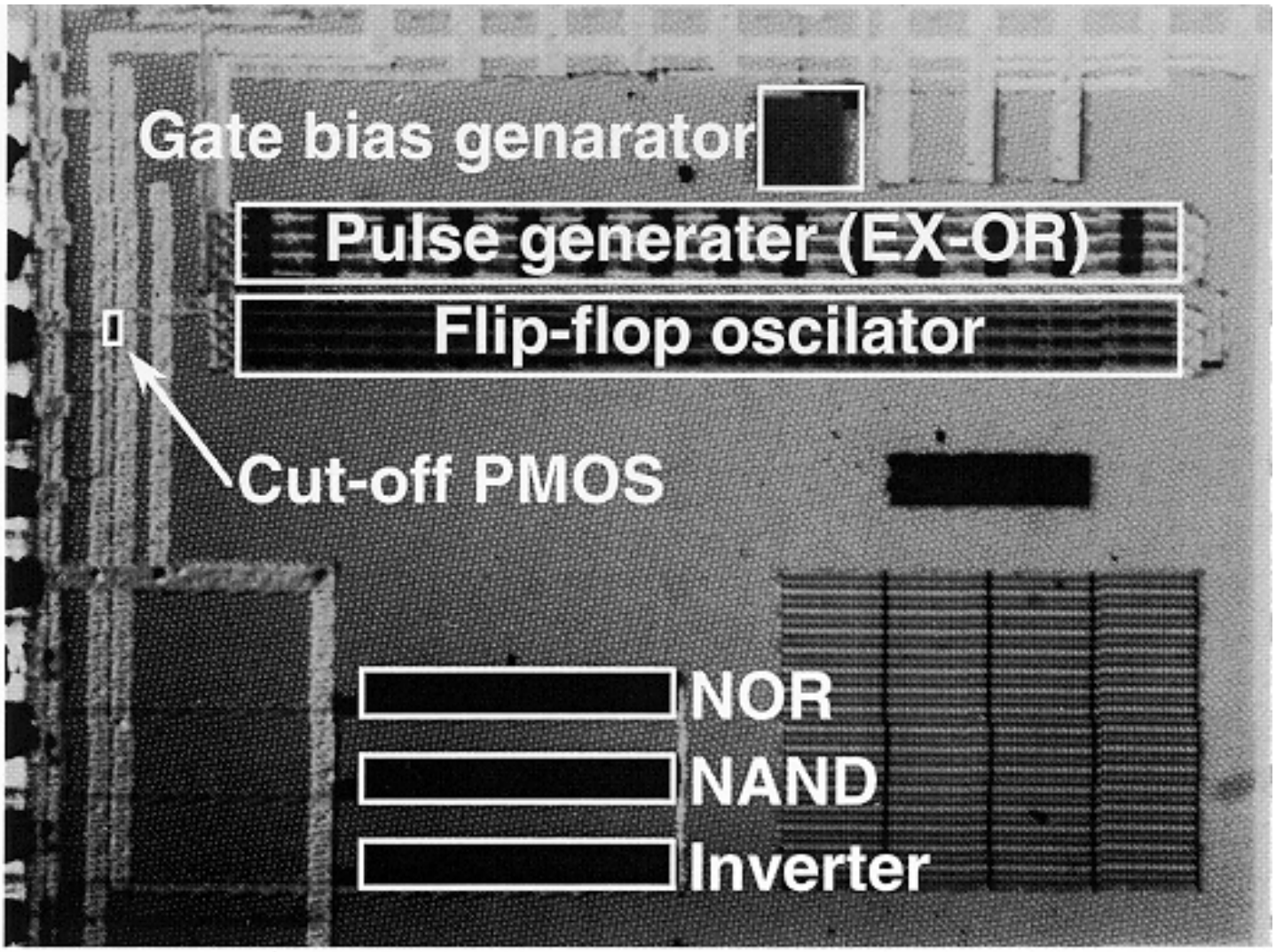

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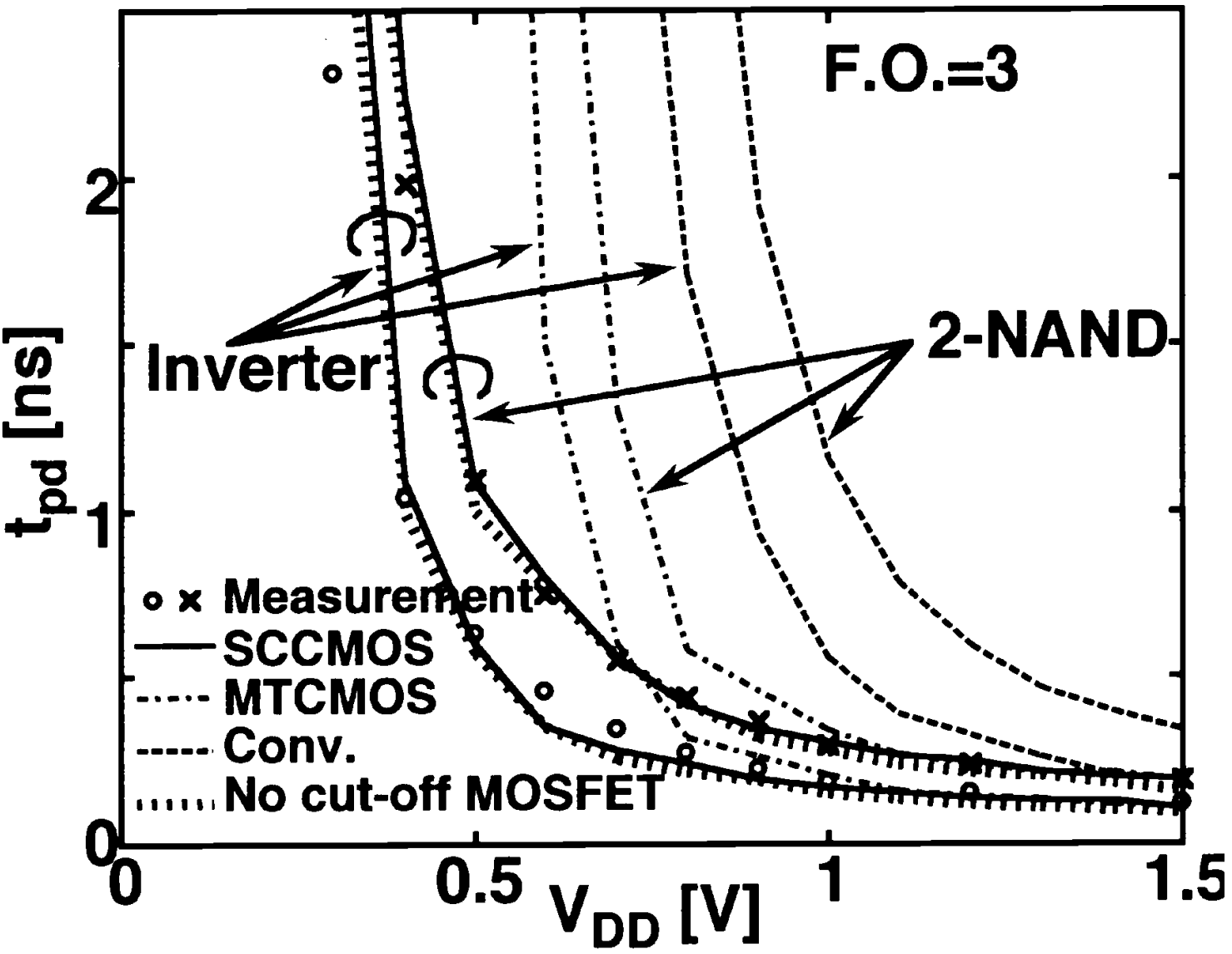

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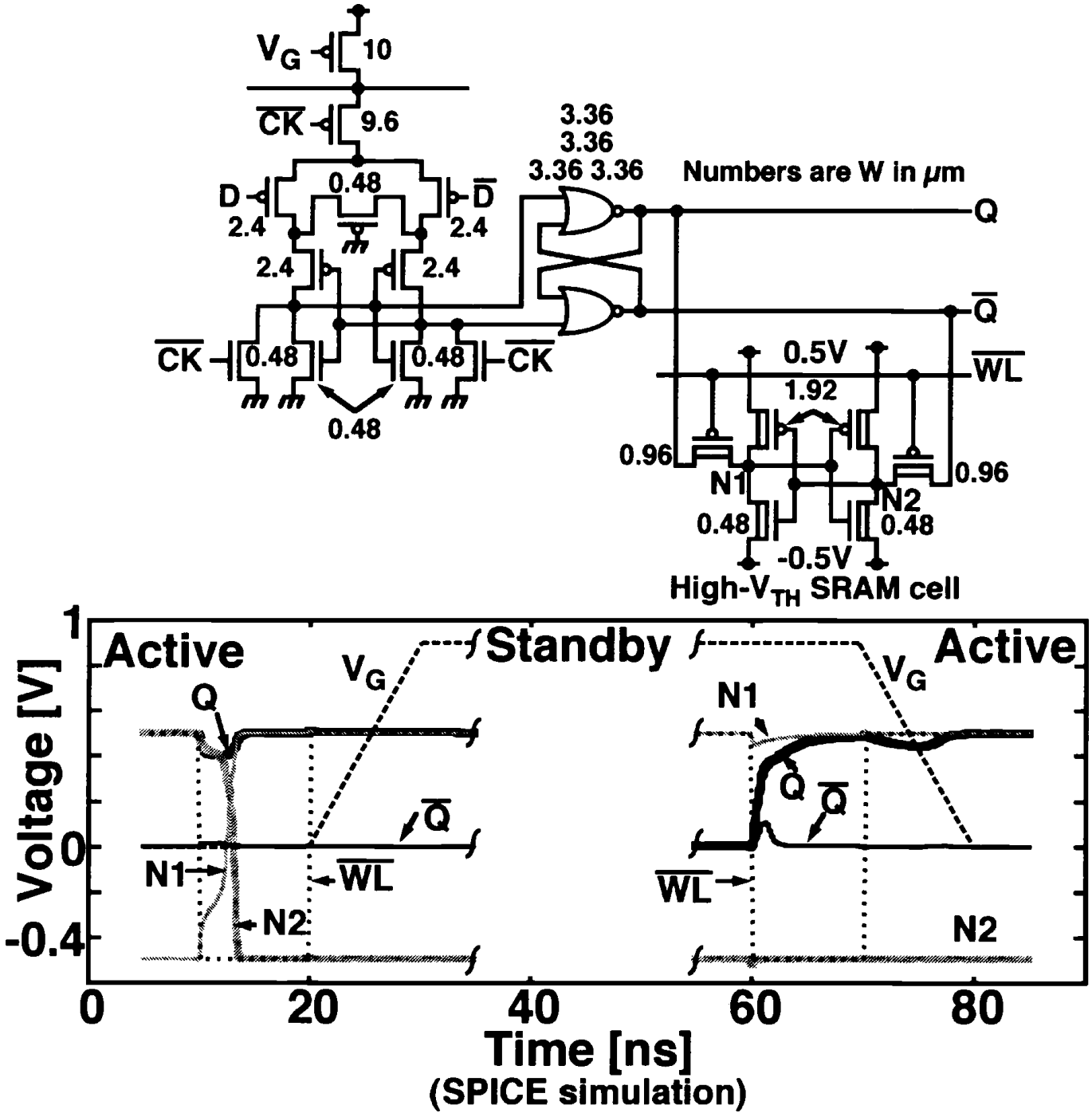

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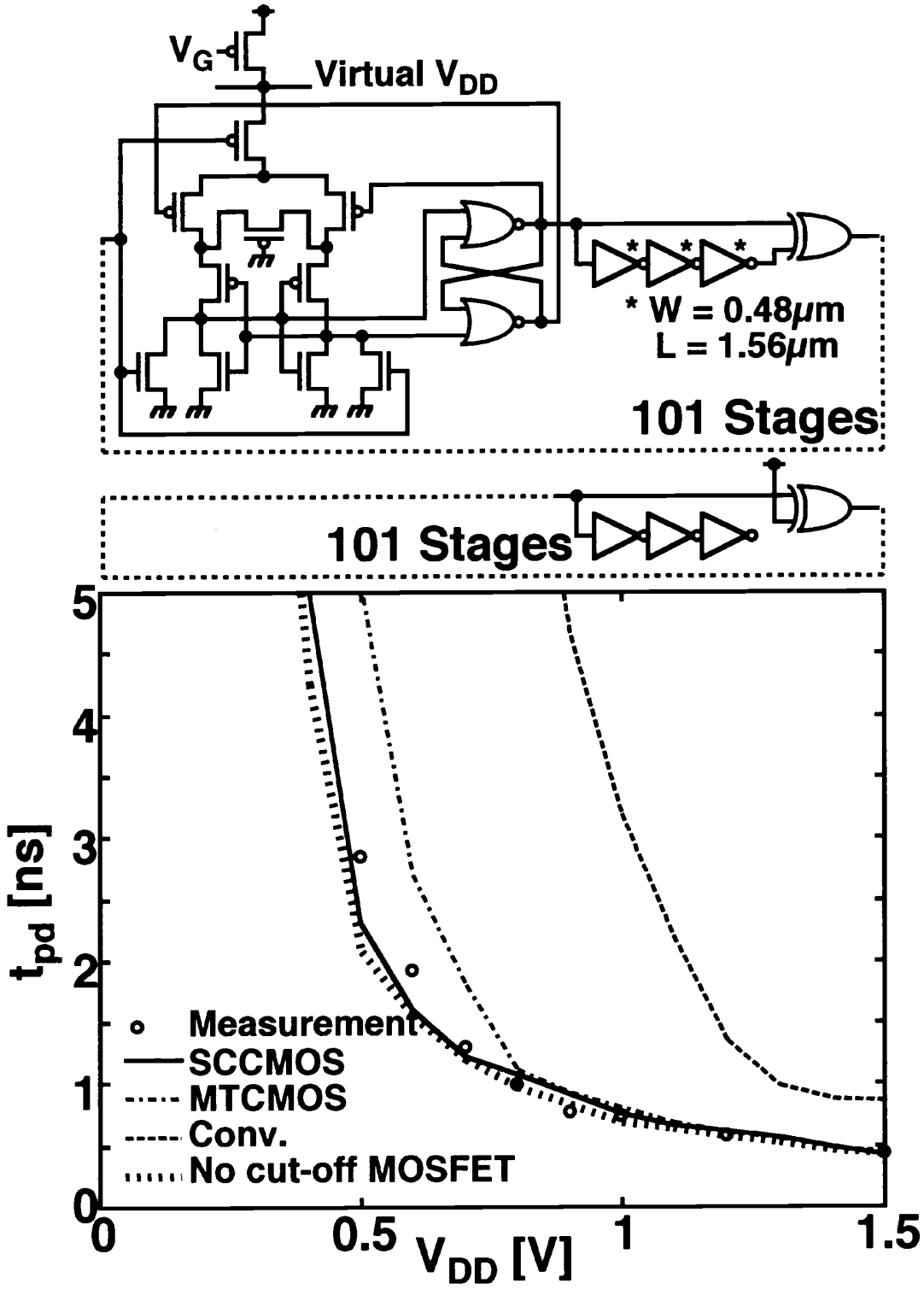

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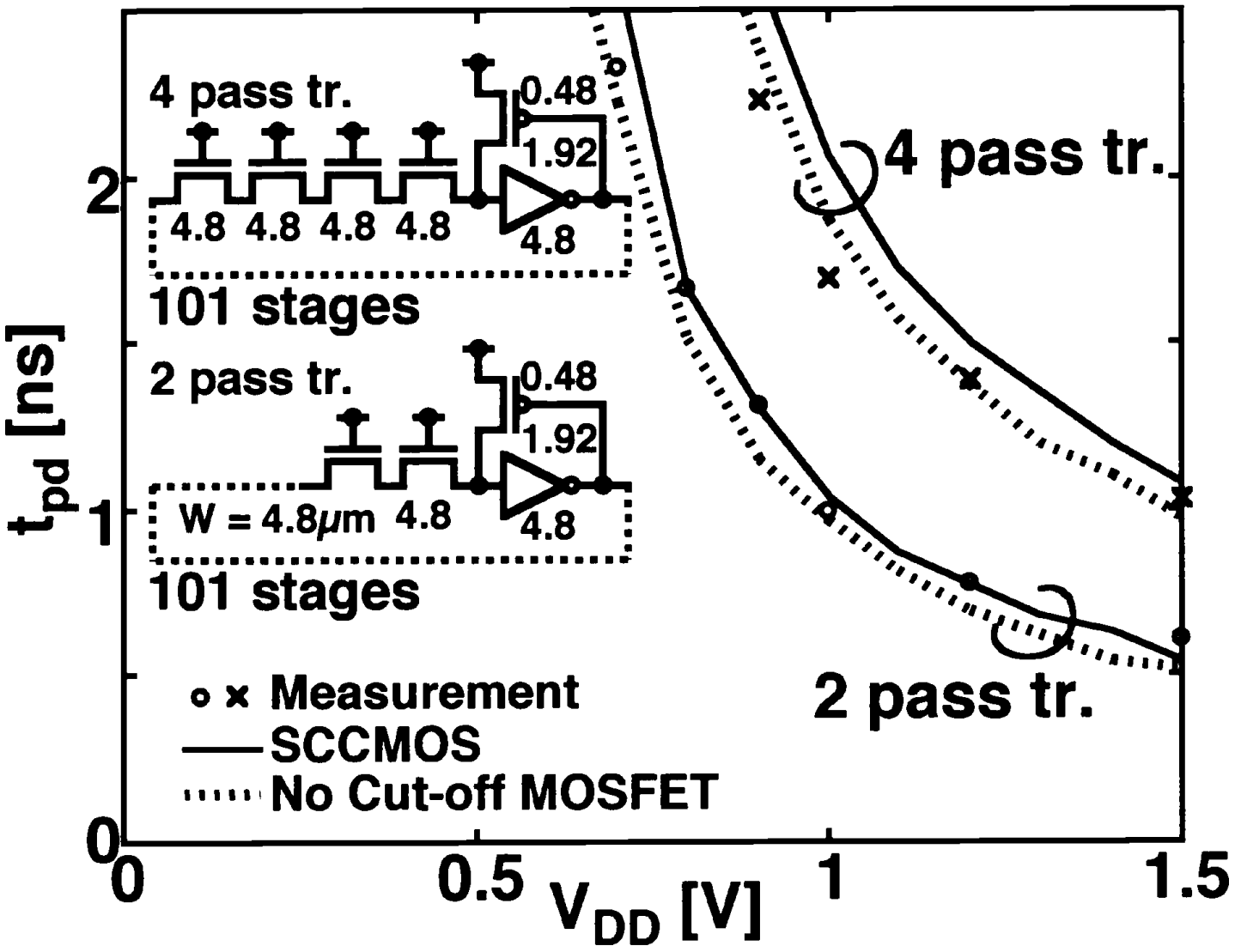
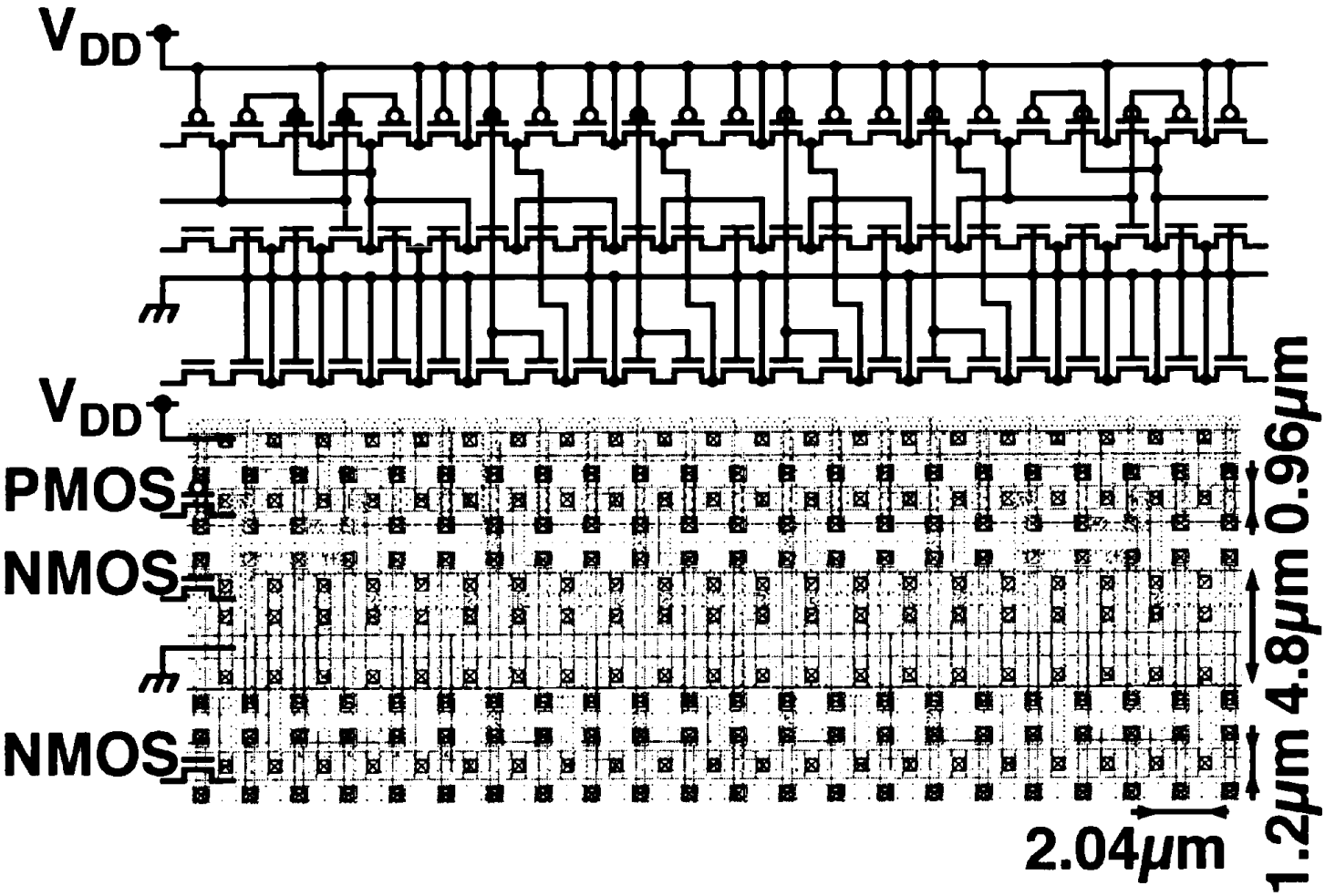


Figure 6: Speed of PTL with SCCMOS.



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