Substrate Noise Influence on Circuit Performance in Variable Threshold-Voltage Scheme

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Abstract - This paper investigates substrate noise influence on circuit performance in a variable threshold-voltage scheme (VT scheme) where threshold voltage is dynamically varied by substrate-bias control to reduce active power dissipation. It is experimentally examined that substrate-bias can be controlled stably with very few substrate-contacts. Measured tracking jitter of a delay-locked loop implemented by interconnections in an 8mm-square gate array does not degrade even when substrate-contacts are removed except for one at every strip of p-sub and n-well. A 2mm-square discrete cosine transform core processor with no substrate-contact except in its periphery operates at supply voltages from 1.3V to above 3V even though it employs small-swing differential dynamic pass-transistor logic. No performance degradation nor latchup is observed in these chips even when 100kΩ resistance is added to the substrate. These experimental results demonstrate noise immunity of the VT scheme, and indicate the possibility that the VT scheme can be applied to existing macro design easily.

I. INTRODUCTION

Lowering both of the supply voltage, V_{DD}, and threshold voltage, V_{th}, enables high-speed, low-power operation. This approach, however, raises three problems; 1) degradation of worst case speed due to V_{th} fluctuation in low V_{DD}, 2) increase in standby power dissipation in low V_{th}, and 3) disablement to sort out defective chips by monitoring the quiescent power supply current (I_{DDQ}).

Two circuit schemes to solve these problems were proposed. One is to employ two V_{th}; low V_{th} for fast circuit operation and high V_{th} for cutting internal power supply voltage in a standby mode [1]. This scheme, however, solves only the standby power problem, and requires very large transistors for the power supply control to impose area and yield penalties, otherwise circuit speed degrades. Furthermore it cannot be applied to memory elements. The other scheme is to dynamically vary V_{th} through substrate-bias, V_{BB} ; hence the name variable threshold-voltage scheme (VT scheme). As illustrated in Figure 1, V_{BB} is controlled so as to compensate V_{th} fluctuations in an active mode, while in a standby mode and in the I_{DDQ} testing deep V_{BB} is applied to increase V_{th} and cut off leakage. Several circuit implementations were developed [2-4]. The VT scheme can solve the three problems all together, requires no large transistor, and can be applied to both logic gates and memory elements. However, it may impose an area penalty for routing the substrate-contacts globally, compared to the conventional layout design where they are connected to power lines locally. Addition of the substrate-contact interconnections makes application of the VT scheme to existing macro design impractical. Without clear understanding of substrate noise influence on circuit performance we cannot figure out how many substrate-contacts we should place and route.

Fig. 1 Variable Threshold-Voltage (VT) scheme.

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Fig. 2 GA chip micrograph.

In order to investigate this issue, two testchips are fabricated in a 0.3μm CMOS technology and intensively examined; a gate array testchip and a discrete cosine transform (DCT) processor testchip. This paper reports the experimental results and discuss substrate noise influence on circuit performance in the VT scheme. Experimental results and discussions with the gate array testchip is presented in Section II and those with the DCT testchip is found in Section III. Section IV is dedicated for conclusions.

II. GA Experimental Results

A gate array chip with the VT scheme is designed which includes available gate counts to 188 thousand on an 8mm die. A chip micrograph appears in Figure 2. Two variants are designed in terms of the number of the substrate-contacts in each strip of p-sub and n-well in basic-cell area; (a) only one substrate-contact at one end of each strip as illustrated in Figure 3(a), and (b) 400 substrate-contacts per strip as depicted in Figure 3(b). In (a) source diffusions are added in place of the substrate-contacts to stabilize V_{BB} by junction capacitance between source diffusions and substrate. Test circuits are implemented by interconnections; a delay-locked loop (DLL), and a 4K-bit SRAM. They are very sensitive to the substrate noise, and therefore, can be good monitors. 64 gate chains are used for a noise source by having them all operate at 50MHz. The monitors and the noise source share the same p-sub and n-well because the well-strip runs vertically in the basic-cell area.

Measured tracking jitters of the DLL with 50MHz input clock at V_{DDL}=2.0V are presented in Figures 4(a) and (b). Two peaks appear in the histogram. This is not due to noise induced error but due to a unique and simple tracking control scheme of this DLL. The peak-

(a) one substrate-contact. (b) 400 substrate-contacts.
Fig. 3 Two variant substrate-contact designs.

(a) one substrate-contact with noise.

(b) 400 substrate-contacts without noise.
Fig. 4 Measured DLL tracking jitter.

Fig. 5 Measured DLL tracking jitter vs. V_{DDL}.

to-peak jitter in (a) one substrate-contact with the noise source is 680ps, while in (b) 400 substrate-contacts without the noise source is 620ps, no big difference between them. Figure 5 summarizes the measurement results of the jitter dependence on V_{DDL} when input clock frequency is 50MHz. Since the measurement is taken on wafer samples through a probe card it receives noise from environments. No clear difference beyond the noise induced error is seen between (a) and (b). SRAM shmoo plots are also taken which appear in Figures 6(a) and (b). The difference is not easily distinguishable. From these measurements it is considered that one substrate-contact per well-strip is enough for making V_{BB} stable.

III. DCT Experimental Results

Another testchip is a discrete cosine transform (DCT) core processor in Figure 7. This executes two-dimensional 8x8 HDTV-resolution video compression and decompression. Original design was made for an n-well technology [5]. We have modified the well/substrate-contact layout for the VT scheme as follows. Firstly have the DCT macro wrapped by deep n-well, secondly generate p-well by inverting n-well data in the deep n-well, thirdly replace all the substrate-contacts by source diffusions if design rules accept, and lastly place substrate-contacts at the periphery of the deep n-well and the p-well. This modification is made automatically by a program in an layout editor tool. As shown in Figures 8 (a), (b), and (c), the p-well becomes one island. The n-well becomes many pieces of separated islands but can be connected by the deep n-well. Therefore, all the p-well and n-well islands can be connected at the periphery of the DCT macro. Triple-well structure prevents substrate noise current introduced from I/O cells from affecting the DCT macro. The increase in cost and turn-around time by introducing triple-well process is less than 5%.

(a) one substrate-contact with noise.

(b) 400 substrate-contacts without noise.

Fig. 6 RAM shmoo plot.

Fig. 7 DCT chip micrograph.

(a) device cross-section. (b) p-well (one island). (c) n-well (pieces of islands) in deep n-well.
Fig. 8 DCT layout modification for the VT scheme so that substrate-contacts are placed only at the periphery.

High-speed but noise-sensitive circuits are employed in the DCT macro such as small-swing differential dynamic pass-transistor logic with sense-amplifying pipeline flip-flop [5], and various memories such as ROM's and SRAM's. The DCT macro, however, operates with 40MHz clock input at supply voltages from 1.3V to above 3V. Even when external resistance of up to 100kΩ is added to the p-well and n-well, no performance degradation nor latchup effect is observed.

IV. Conclusions

Noise immunity of the VT scheme is demonstrated. Substrate-bias is stable with very few substrate-contacts. The number of a dynamic node (propagating signal) is much fewer than that of a static node (staying "H" or "L") at a moment. It is considered that parasitic capacitance between substrate and diffusions of the static nodes works effectively to stabilize substrate-bias against high frequency noise. Simultaneous switching of large number of data bath at local area, however, should be treated with care. Since substrate current generation due to the impact ionization is a function of the supply current, lowering the supply voltage eases latchup problem.

Acknowledgment

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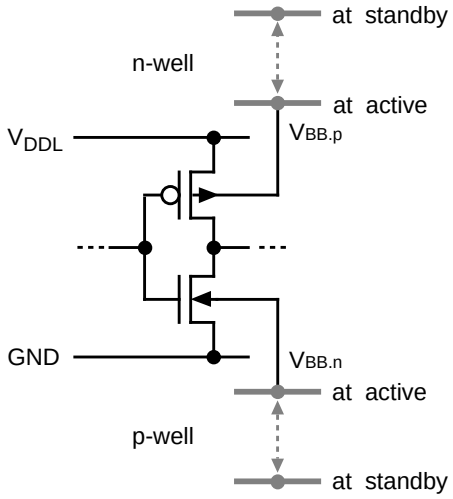


Fig. 1 Variable Threshold-Voltage (VT) scheme.

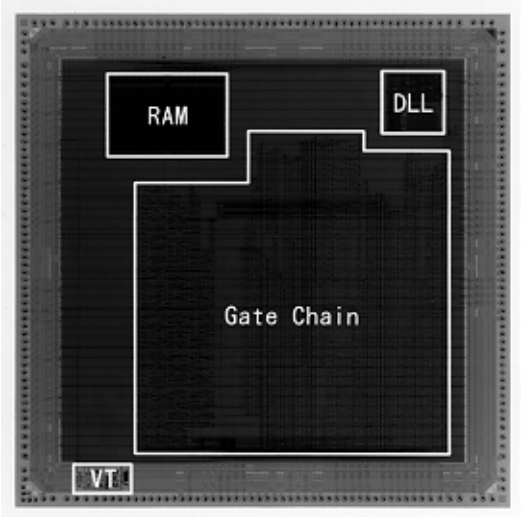
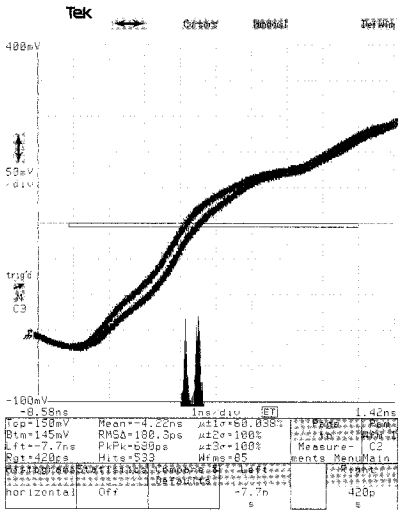
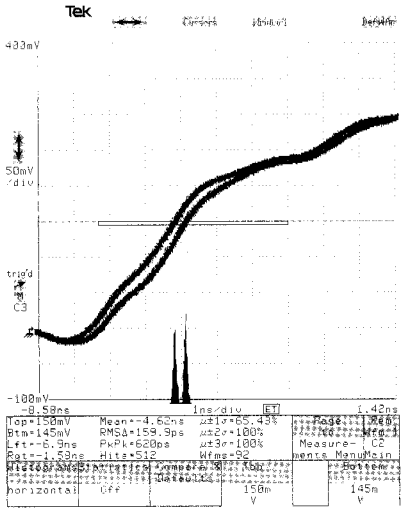


Fig. 2 GA chip micrograph.

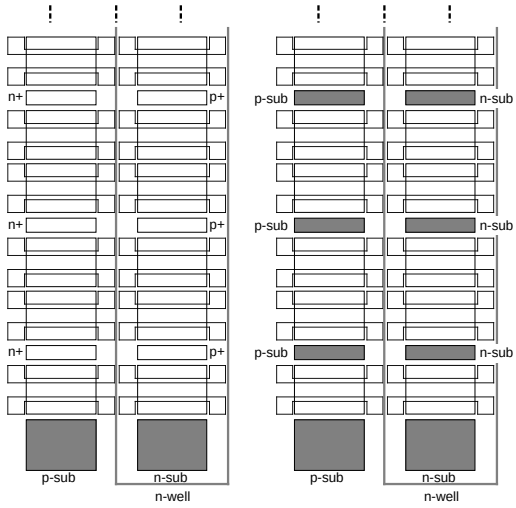


(a) one substrate-contact with noise.



(b) 400 substrate-contacts without noise.

Fig. 4 Measured DLL tracking jitter.



(a) one substrate-contact. (b) 400 substrate-contacts.

Fig. 3 Two variant substrate-contact designs.

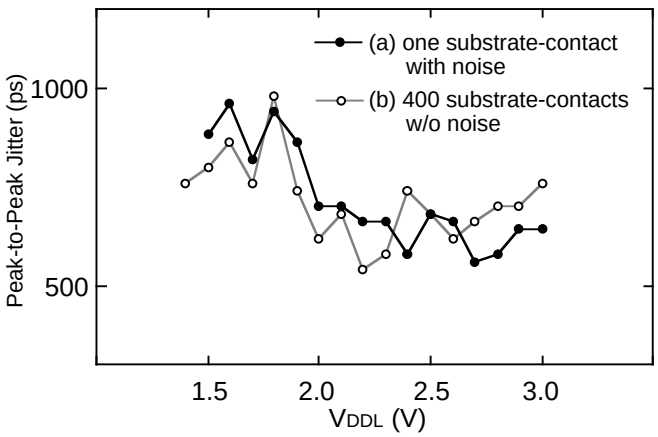
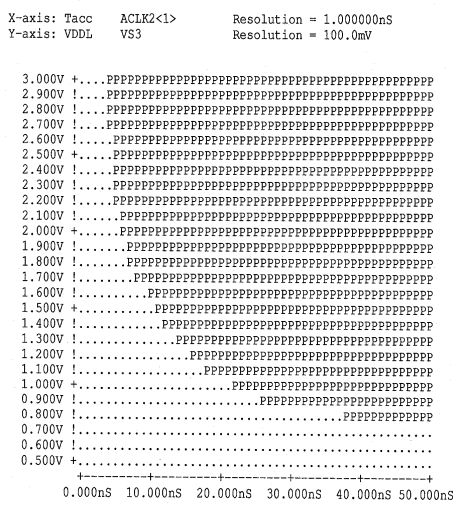
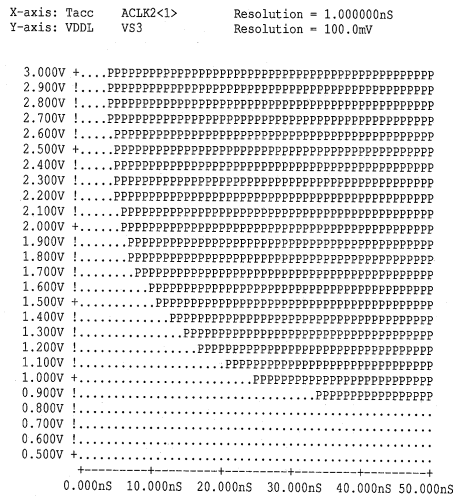


Fig. 5 Measured DLL tracking jitter vs. V_{DDL}.



(a) one substrate-contact with noise



(b) 400 substrate-contacts w/o noise

Fig. 6 RAM shmoo plot.

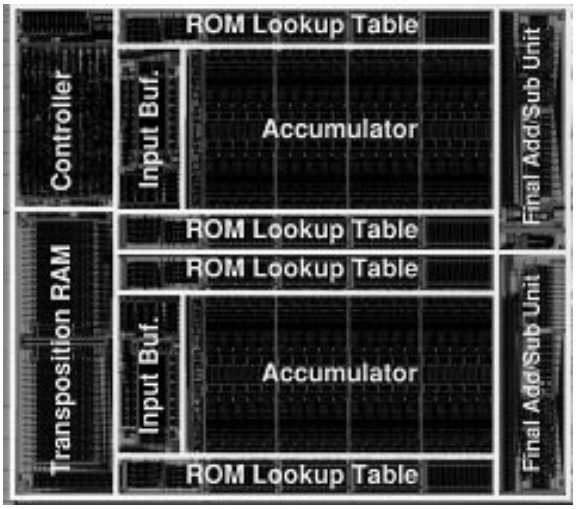
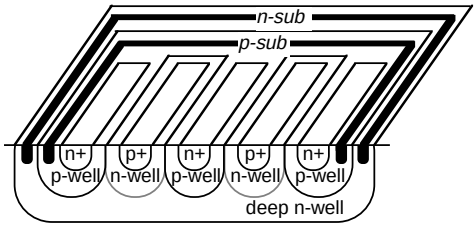
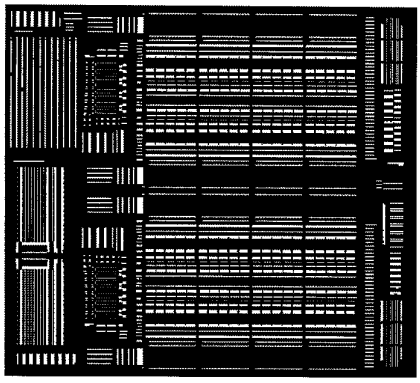


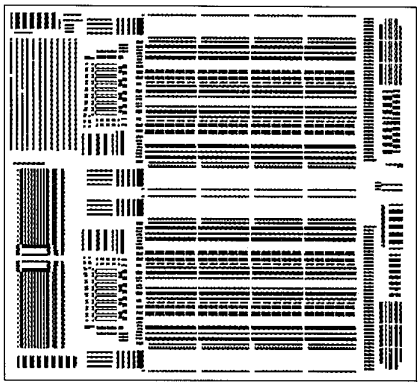
Fig. 7 DCT chip micrograph.



(a) device cross-section.



(b) p-well (one island).



(c) n-well (pieces of islands)in deep n-well.

Fig.8 DCT layout modification for VT scheme so that substrate-contacts are placed only at the periphery.