Evening Rump Sessions

R1 Future High Performance Microprocessor Implementation Tradeoffs

Moderators:	I. Young	Intel
	T. Sakurai	Toshiba

In designing future microprocessors for higher performance, the circuit designer is being challenged to maximize the performance derived from additional transistors and higher clock rates. What are the new circuit micro-architectures and features that will provide increased performance and functionality in this context? Will the die area and power consumption required to implement these be cost effective and practical?

R2 Flash EEPROM: A Challenger to DRAM

Moderators:	C. Kuo	Motorola
	Y. Terada	Mitsubishi Electric

Flash EEPROM has the potential of replacing DRAM in many applications. High density, high throughput, low cost and high endurance are key factors to be considered for DRAM applications. This panel discusses cell structures, array architecture, and circuit design techniques for high data throughput and single supply low voltage operation, which are critical to flash EEPROM performance and density. The panel also addresses the issue of maximizing the match between system performance requirements and flash memory performance in order to expand flash EEPROM applications.

R3 Low Power/Low Voltage Technologies: A Joint Circuits & Technology Session

Moderators:	W. Bidermann	HaL
	Y. Nakagome	Hitachi
	N. Lu	Etron

Along with the ability to produce quarter and tenth micron geometry in silicon chips will come increased impact on circuit design. Larger spreads in device characteristics, lowered supply voltages for reliability, process changes for low power applications - these and other considerations will require adaptation in designs which use these advanced processes. This panel of process technologists and circuit designers will address process technology and circuit design tradeoffs for these advanced processes.