EVENING RUMP SESSIONS

R-1 Interfacing of High Speed Logic and Memory

Moderators: S. Schuster, *IBM*
N. Lu, *Etron*

Rapid advances in technology and design have resulted in microprocessors with greater than 200 MHz clock rates and several hundred I/O. In this high speed environment the reliable transmission of signals between logic and memory is a fundamental requirement. The problem is further exacerbated by the widening gap between processor and memory performance. This panel will address the following issues:

- What is the most effective system partition–cache on logic and/or cache on memory. . .? How does this affect the interface design between logic and memory? Are there differences between low-end and high-end PC/WS systems?
- Is a new interface needed? Why? If yes, what is it—GTL, small-swing differential signals, Rambus, center-tapped termination. . . ? Should there be one unified standard interface?
- Implementation issues
  - Technology dependency-CMOS versus BiCMOS
  - Power supply voltage scaling
  - Signal-to-noise ratio with any new interface
  - Other concerns such as cost, power, speed . . .

R-2 Multi-Million Gate ASIC's

Moderators: T. Sakurai, *Toshiba*
A. El Gamal, *Stanford Univ.*

The era of multi-million gate chips is approaching. The ASIC design methodology where designs are built out of reusable libraries is fast becoming the methodology of choice for designing system-level VLSI's. There are, however, a number of competitive ASIC solutions. The rivalry between gate arrays and standard cells is well known and still persists. Serious competition from embedded arrays threatens to obsolete standard cell. But will it? What about FPGAs? Can they compete in the million-gate arena? Will they only be used to prototype or emulate such large designs? Will these competing approaches co-exist or will some dominate the scene.

Manufacturing a million-gate ASIC can be done today. The question is can today's design tools handle such designs. Clock distribution, power/ground distribution and noise problems are some of the issues that remain to be solved. What about synthesis and verification tools? Can they handle such complexity?

Although at present, the Sea-Of-Gates architecture using a 4 transistor cell dominate. Will it be adequate for future generations?

Power management circuitry and testability circuitry, should they be left to designers or should they be added to the base array?

How will Multi-Million gate ASICs be packaged? Will multi-chip modules play a role? As for high-speed designs, are BiCMOS, ECL and/or on chip Phase-Lock-Loop effective solutions? Will reduced swing I/O's become main-stream?

The main objective of the session is to discuss these problems and potential solutions for realizing future multi-million gate ASIC's.

R-3 Ultra Low Power Circuit Design and Technology

Moderators: K. Asada, *Univ. of Tokyo*
W. Bidermann, *DEC*
R. Brodersen, *Univ. of California at Berkeley*

The requirements of portability are driving the power supply voltages ever lower. In order to retain performance, it is desirable to lower the thershold voltage which is ultimately limited by subthreshold conduction. A variety of circuit and process technology design solutions to this problem will be discussed including such techniques as direct sensing of subthreshold current, series resistance, switched supplies as well as process optimization for low voltage operation.