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Transparent-Refresh DRAM (TReD) Using Dual-Port DRAM Cell

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Abstract

A new memory circuit, namely Transparent-Refresh DRAM (TReD), is proposed to make a dynamic RAM virtually refresh-free, and a test device is successfully fabricated. The TReD uses dual-port dynamic RAM cells, one port of which is assigned for a refresh operation and the other port is assigned for a normal read/write operation. Thanks to this configuration, users of the RAM are freed from a cumbersome refresh control without any normal access time degradation. The TReD cell size is about 1/2.5 of 4-transistor SRAM cell, so that it can provide very high-density RAM macros, which is functionally static. As a dual-port memory, the proposed dual-port DRAM cell size is 1/5 of the dual-port SRAM cell, and is suitable for a large scale dual-port memory macros in ASIC environments.

I. Introduction

A dynamic RAM (DRAM) has storage density four times as high as a static RAM (SRAM). For this advantage, DRAMs are frequently used in a large scale memory system. DRAMs, however, require complex refresh controls for data retention, which is one of the main reasons why users prefer SRAMs to DRAMs, especially in small systems. Recently, several attempts have been made to free the DRAM users from cumbersome refresh controls[1,2,3,4,5], namely a pseudo static RAM (PSRAM) and a virtually static RAM (VSRAM). The PSRAM[1] can sustain stored data without refresh control on user's side in stand-by mode. However, in active mode, the PSRAM requires refresh operation triggers from user's side and in this refresh operation an arbitration is required between a normal access and a refresh operation, which may cause about three times longer access time than an access time without the arbitration. The VSRAM[2,3,4], on the other hand, entirely frees the users from refresh controls with an aid of an on-chip arbiter. However, the access time of the VSRAM is much longer than a normal DRAM, say 1.8 times longer, because a normal access operation might wait until the internal refresh ends when the refresh takes place in advance to the normal operation. Another approach[5] is based on a 4Tr dynamic cell. Although no additional access time is required in this approach, the cell size is almost as large as the convention 4Tr SRAM cell and the most attractive high-density feature of the DRAM cell is lost.

This paper proposes a new approach to a virtually static RAM, namely Transparent-Refresh DRAM (TReD). Using dual-port DRAM cells, the TReD provides both of the high-density feature and the fast memory access time. The memory cell size of the TReD is smaller than the conventional SRAM and the access speed is faster than that of the PSRAM and the VSRAM. This is because, in the TReD, the internal refresh takes place completely in parallel with the normal operation as a background job, thanks to the dual-port configuration. The RAM is suitable for a RAM macro in ASIC environments, where critical timing control of a refresh is impossible because of a CAD limit.

Section II describes the TReD concept. Key design considerations are discussed in Section III. In Section IV, the feasibility is verified by a test device. Section V and VI are dedicated to discussions and conclusions, respectively.

II. TReD Concept

The memory cell of the TReD consists of two transfer-gates and one capacitor as is shown in Fig.1(b). Two word lines, namely Normal Word Line (NWL) and Refresh Word Line (RWL) and two bit lines, namely Normal Bit Line (NBL) and Refresh Bit Line (RBL) are connected to one memory cell. Owing to this dual-port configuration, a refresh operation using RWL and RBL can be carried out completely in parallel with a normal access operation using NWL and RBL. So that no access time overhead is required. With an on-chip refresh controller which triggers refresh operations at adequate periods, the TReD cell looks like a 'static' RAM from a normal port, because the TReD cell restores decayed charge from a refresh port. In this way, the refresh is completely transparent to the users of the normal port.

As for a layout of a memory cell, the dual-port DRAM cell is constructed by merely merging two adjacent cells of the conventional DRAM cells. Therefore, the TReD requires no additional process technology over a DRAM process. Since the TReD can be made even with trench-type memory cells, the memory capacity can well exceed 1Mbit level[6].

III. Design Considerations

a. Read Operation

In the TReD, cell capacitance should be twice as large as that of the conventional DRAM. This is because in the TReD, two word lines (NWL and RWL) can be opened

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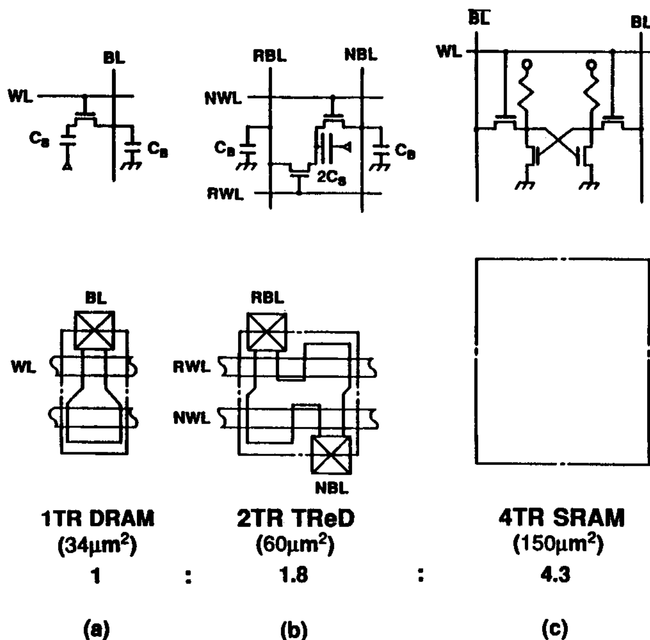

Fig.1. Comparison of (a) 1Tr DRAM cell, (b) 2Tr TReD cell, and (c) 4Tr SRAM cell

at the same time and then the effective bit line capacitance is twice as large as in the case of the conventional DRAM. In order to maintain bit line signal voltage at the same level as in the conventional DRAM, the cell capacitance of the TReD should be twice as large as that of the conventional DRAM. Consequently, the TReD 2Tr cell occupies 1.8 times larger silicon area compared to the conventional DRAM[7]. However, this area is about 1/2.5 of 4Tr SRAM cell area[8] as shown in Fig.1.

B. Write Operation

When a normal write operation occurs on a cell which is under refresh operation through the other port and a write data is different from a stored data, a contention occurs between the data latched in a refresh sense amplifier and the write data. This contention makes the cell node voltage intermediate between V_{CC} and V_{SS} and causes the data destruction. There are two ways to prevent the data destruction.

First way is to insert a bit line short circuit between NBL and RBL, as is shown in Fig.2(a). NBL-RBL short signal WE^* is generated when the refresh address and the normal write address are the same and NE (Normal Enable) and RE (Refresh Enable) are asserted. Then the refresh sense amplifier flips to the write data and the contention is resolved.

The other way is to shut off the refresh word line and stop the refresh operation when the contention occurs. The refresh operation is not necessary when the refresh row is the same as the normal write row. This is because the non-written cells in that memory row are refreshed through the normal access. This circuit scheme is shown in Fig.2(b).

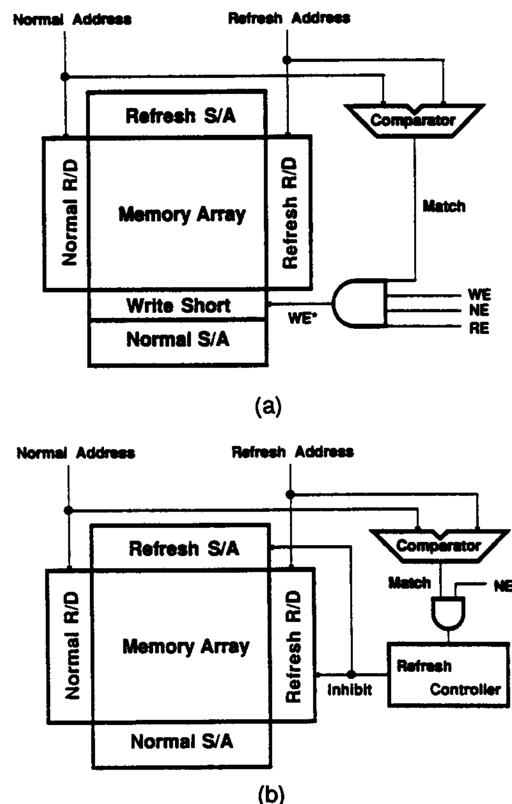

Fig.2. Two circuit schemes for preventing a write-refresh contention.

IV. Test Device Measurements

The feasibility of the above mentioned TReD concept is verified using an experimental device including 1.7K memory cells whose microphotograph is shown in Fig.3. Figure 4 is a micro-photograph of the TReD 2Tr memory cell. The device is fabricated with 1.2μm double-Al double-poly CMOS technology which requires only three extra masks over the standard logic process. Capacitor oxide thickness is 12nm and the cell size is 7.2 x $8.3\mu m^2$. The cell capacitor is planar-type and $2C_S$ = 80fF. Worst-case bit line signal factor $2C_B$ / $2C_S$ equals 15. The dual-pot cells of the test device are embedded in a p-well for protection from the disturbance of logical circuits, so that the resulted RAM can be stable in ASIC environments[11].

Figure 5 and 6 show the circuit diagram and the rough signal waveforms of the memory core part of the TReD. The write scheme adopted in the test device is the first scheme as shown in Fig.2(a). The signal waveforms shows the read-modify-write operation when the normal access cell and the refresh cell are the same, that is, the contention occurs. Figure 7 is measured waveforms of the TReD test device. The rough signal waveforms shown in Fig.6 corresponds to measured wave forms in Fig.7(a). As seen from the figure, "1" and "0" read operation is successfully done even if the refresh and normal read operation are carried out simultaneously for the same cell, that is, NWL and RWL of the accessed cell are opened at the same time.

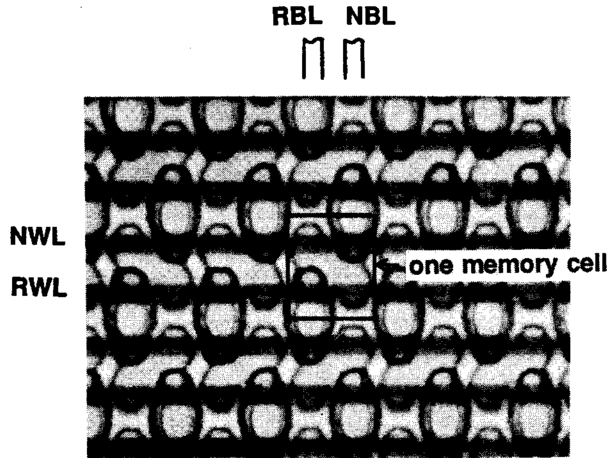

Fig.4. Micro-photograph of dual port DRAM cell before Al metallization.

Thanks to the NBL-RBL short circuit, "1" and "0" write operation can be done even if the refresh sense amplifier latches the previous data (Fig.7(a)). Without the NBL-RBL short circuit, "1" write was failed as shown in Fig.7(b) because the refresh sense amplifier could not flip.

V. Discussions

For clarity, differences between TReD and other RAMs are listed in Table I. DRAM cells may be thought essentially weak and unstable and can not be used in noisy ASIC environments but it has been shown[11] that the well designed DRAM is stable and fully functional even in tough environments. As a RAM macro, virtually static feature is crucially important because the present ASIC CAD tools can not support a critical timing circuit design like refresh controller. In static RAM macros, the TReD has a good mix of high-density and high speed feature. The TReD is the faster compared with a pseudo and a virtually static RAM, because PS/VSRAM require the arbitration between a normal access and a refresh operation with an off-chip or on-chip arbiter, which causes the access time degradation.

The table even indicates that the TReD has a possibility to substitute high-density SRAMs in commodity SRAM market. Usually the speed of high-density SRAMs is comparable to that of fast DRAMs. Since the speed of the TReD is comparable to that of the fast DRAMs, the chip size advantage over 4Tr SRAM makes the TReD an attractive alternate of a commodity high-density SRAM. The performance of the TReD other than speed such as data retention current is also comparable to the conventional SRAM. So that the TReD in standard SRAM market covers large application area such as portable equipments, computer peripherals, buffer memories, and battery backup use.

When the proposed dual-port DRAM cell is used as a normal dual-port memory cell, the cell is suitable for a large scale register file and/or a cache memory system[9,10] since the cell size is 1/5 of the dual-port SRAM cell.

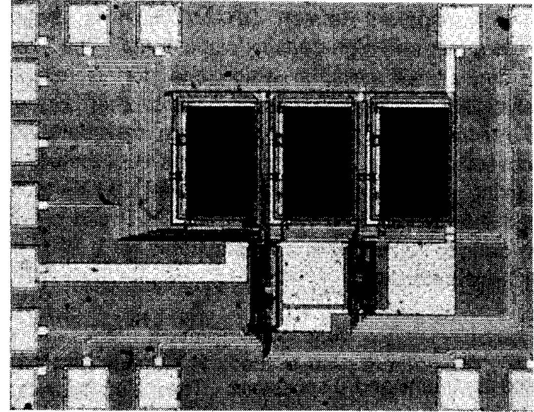

Fig.3. Micro-photograph of test device.

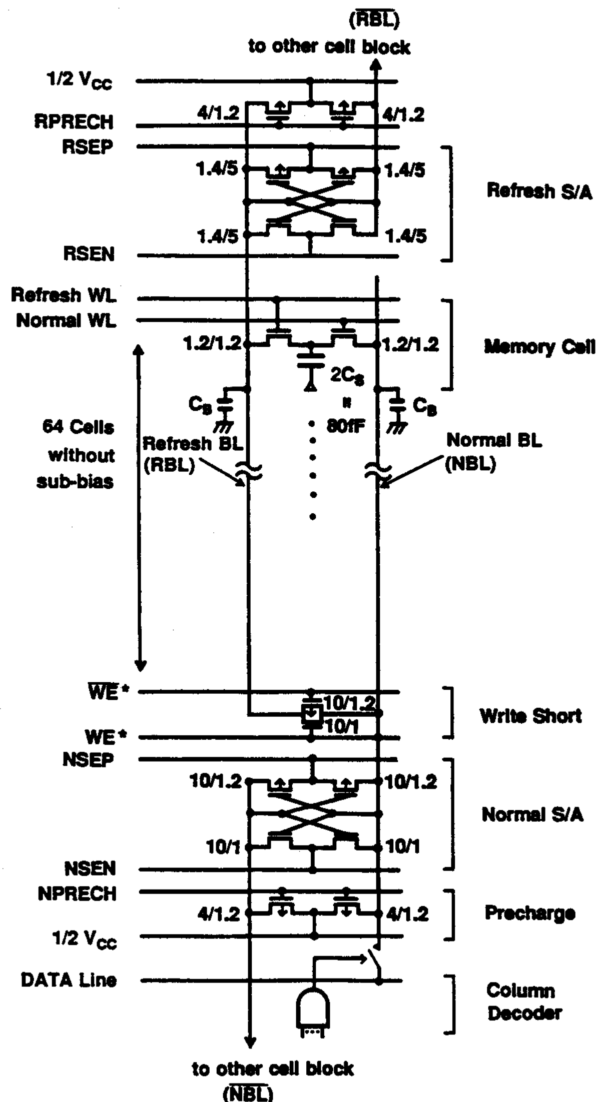

Fig.5. Circuit diagram of TReD memory core part.

VI. Conclusion

Transparent-Refresh DRAM(TReD) is proposed to realize a fast and high-density 'static' RAM. The TReD uses dual-port DRAM cells, in which one port is assigned exclusively for a refresh operation and the other port for a normal read/write operation. Key design considerations were discussed in detail. A test device was successfully fabricated using 1.2μm double-Al double-poly CMOS technology, and the feasibility was verified. The TReD can provide very high-density static RAMs and is suitable for a RAM macro in ASIC environments.

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Table I. Comparison between TReD and other RAMs.

	DRAM	Pseudo SRAM	Virtual SRAM	TReD (This Work)	High-density SRAM
Chip size	1	1.1	1.1	2	4
Access time	80ns	80ns	150ns	80ns	70ns
Data retention current	1mA	100μA	100μA	100μA	100μA
Refresh	user control	user control	free	free	free

Note1 : Assuming 1Mbit capacity and 1.0μm CMOS process.
Note2 : Values are estimated specification values.

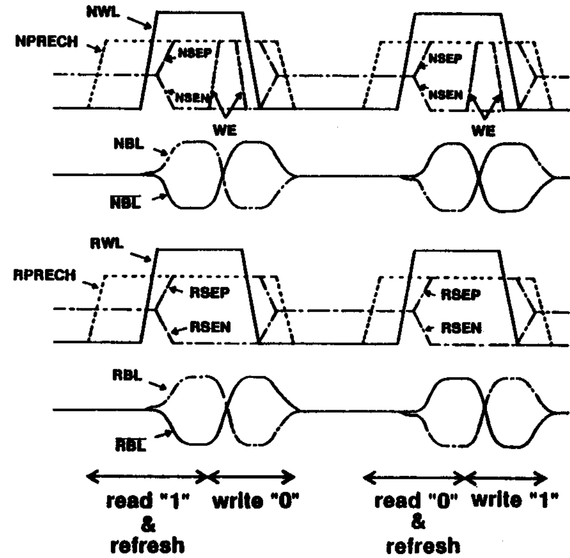

Fig.6. Rough operation waveforms of TReD.

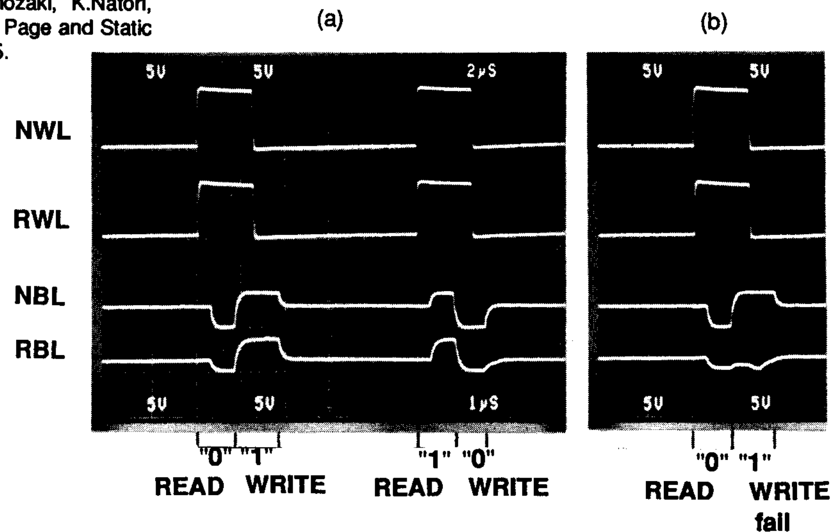

Fig.7. Measured waveforms of TReD. (a) "0" & "1" READ and WRITE operation is successful when NBL-RBL short circuit is active. (b) "1" write operation fails when NBL-RBL short circuit is inactive.