SESSION XVIII: MODELING AND TECHNOLOGY

FAM 18.7: Hot-Carrier Suppressed VLSI with Submicron Geometry

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RELIABILITY DEGRADATION of small geometry MOSFETs due to hot carriers is one of the most serious problems that prevail for high speed and high density VLSIs. It is known[1] that the threshold voltage shift and conductance degradation are closely related to the substrate current that serves as a good monitor of the amount of generated hot carriers. Continuing efforts are being made to characterize degradation by dc measurements and also ac measurements of n-ch inverters[2]. This paper will describe a substrate current circuit simulator, applied to CMOS unit circuits and CMOS VLSIs. It was found that Vgs-Vds trajectory control is effective to improve circuit reliability. Circuits to suppress the hot carrier generation will be proposed. Many VLSI design implications have been obtained by the analysis, and applied to actual VLSI designs.

The substrate current model is basically a combination of earlier models[3], modified to include substrate bias effects in the form of Taylor's expansion, which is shown in Figure 1 with a concrete expression. Previous models failed to reproduce V_{bs} effects. Matching of the measured results for a 1.0μ gate LDD MOSFET to model calculation was very good. Fitting was also successful down to the 0.8μ gate length conventional device with an oxide thickness of 16nm.

Figure 2 offers a comparison between simulated and measured substrate current waveforms for a CMOS inverter consisting of 1μ MOSFETs. The agreement was satisfactory. Figure 3 shows dependence of the substrate current of an inverter on load capacitance. The V_{gs}-V_{ds} trajectories with the constant substrate current plot in Figure 4 illustrates this dependence. It should be noted that the substrate current of a typically-loaded circuit, generated by a falling step voltage, is negligibly small (by over two orders of magnitude) compared with a rising step, and thus, lower load capacitance is preferable.

NAND circuits (Figure 5*a*) offer improved characteristics over inverters and OR gates. The serial connection of n-ch MOSFETs relaxes drain voltage of each MOSFET and hence hot carrier generation, especially when input I2 changes after input I1 rises. For logic VLSI, a NAND-rich technique is recommended. Similarly, the clocked CMOS (C^2MOS) in Figure 5*b*, where the clock comes after input signals settle, generates less hot carrier than a transmission gate in Figure 5c by a factor of a hundred. A normally-on MOSFET inserted at the top of n-ch logic (Figure 5*d*) also improves the duty ratio by two orders of magnitude. The operation of this circui at 5V is faster than that of normal inverters operated at 3V by a factor of 10-40%, depending on the logic configuration. This method is applicable to submicron VLSI unit gates or sen: amplifiers. A Limited Voltage Swing Buffer (Figure 5e), affor smaller substrate current – two orders of magnitude – and over 20% faster speed, than a conventional buffer at the same operation voltage, because the voltage swing of the large capacitance line is limited to about 3V.

Application to VLSI static RAM[4] is illustrated in Figure 6. Simulated duty ratios are shown for heavily loaded bus drivers. Typical value is 1%, which is smaller than a ratio of signal transient time to a cycle time by a factor of about ten. The most dangerous MOSFET is a transfer gate of a memory cell when read "0" operation takes place. Applying lower voltage to a bit line helps to decrease substrate current drastically without degrading bit line speed[5]. The duty ratio for the memory cell transfer gate can be reduced by shorter word line delay.

The data presented are also valid for CMOS dynamic RAM peripheral circuits. In addition, the half Vcc precharge for bit lines improves the duty ratio of a memory cell by more than two orders of magnitude, compared with a Vcc precharge method. Bootstrapped row decoders are safe in terms of substrate current.

The amount of generated hot carrier in submicron VLSI environment can be reduced by careful design considerations based on circuit physics of substrate current. These procedure have been applied to 256Kb CMOS static RAM[4] design, and as a result no performance degradation was observed after 1000hr. accelerated high-voltage stress tests.

Acknowledgments

The authors wish to thank M. Isobe, J. Matsunaga, K. Hashimoto, T. Ohtani, K. Tamaru, M. Saito, K. Sawada, M. Kinugawa, for valuable discussions and support in the computation and measurements.

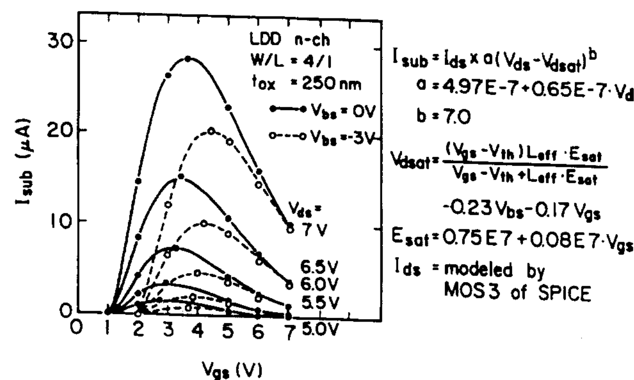

FIGURE 1—Numerical model of substrate current.

[1] Takeda, E., et. al., "Hot-Carrier Effects in Submicron VLSIs", *Symp. on VLSI Tech.*, p. 104; 1983.

[2] Hsu, F.C. and Chiu, K.Y., "Hot-Electron Substrate Current Generation During Switching Transitions", *Symp. on VLSI Tech.*, p. 86; 1984.

[3] Sing, Y.W. and Sudlow, B., "Modeling and VLSI Design Constraints of Substrate Current", *IDEM*, p. 732-735; 1980. Hu, C., "Hot Electron Effects in MOSFETs", *IEDM*, p. 176-181; 1983.

[4] Sakurai, T., et. al., "A Low Power 46ns 256Kb CMOS Static RAM with Dynamic Double Word Line", *IEEE J. SSC SC-19*, No. 5; Oct., 1984.

[5] Sakurai, T., Sawada, K., Iizuka, T., "VLSI-Oriented Voltage Down Converter with Sub-Main Configuration", *Int. Conf. on Sol. St. Device and Materials*, LC-1207; 1984.

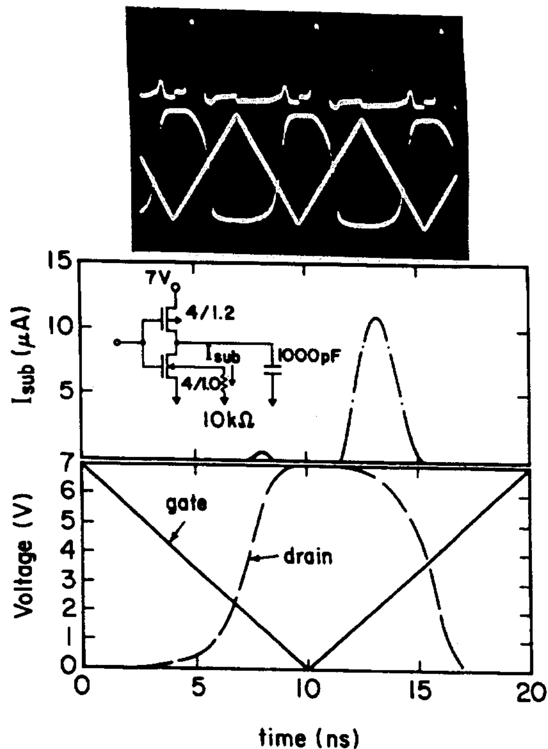

FIGURE 2—Substrate current waveforms of an submicron inverter: (*a*) measured waveform including charging-discharging current of capacitances which is not hot, (*b*) simulated.

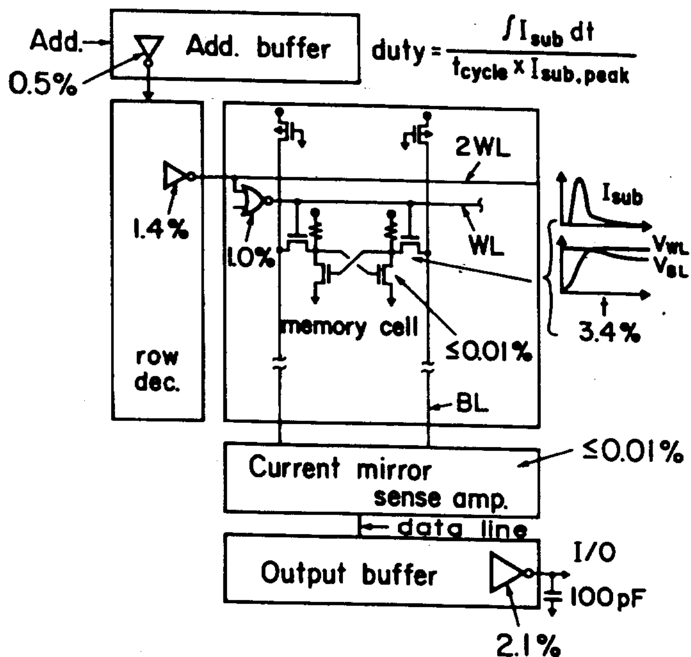

FIGURE 6—Hot carrier duty ratios for 256Kb CMOS SRAM.

[Right]

FIGURE 5—Calculated duty ratios in typical (*a*)—NAND gate, (*b*)—C²MOS gate, (*c*)—transmission gate, (*d*)—normally-on MOSFET inserted gate, (*e*)—limited voltage swing buffer.

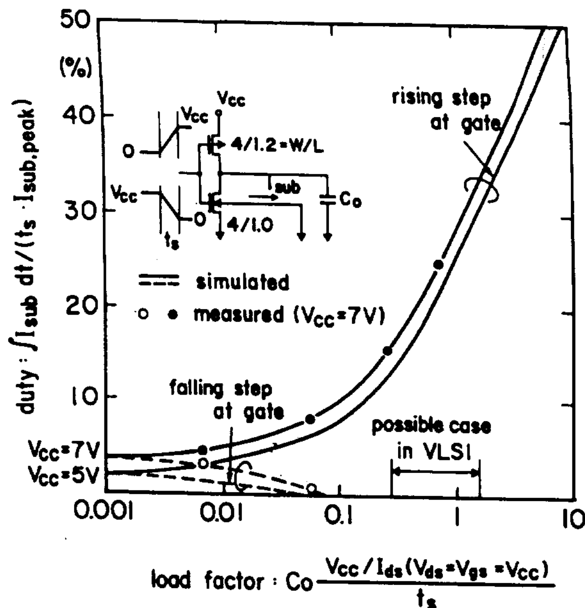

FIGURE 3—Substrate current for various load conditions.

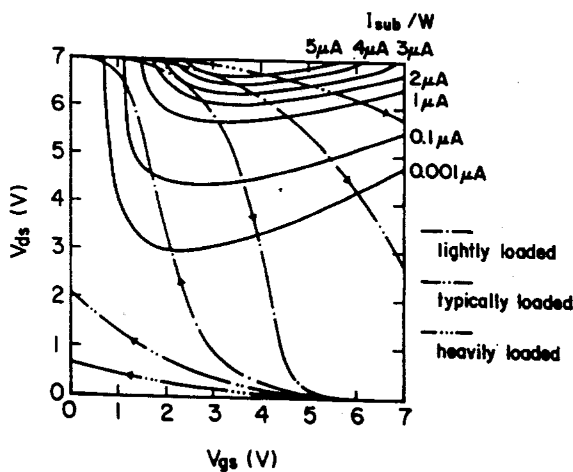

FIGURE 4—V_{gs}-V_{ds} trajectories of CMOS inverters and equi-Isub plot.