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CR ISOLATED CELL FOR SOFT ERROR PREVENTION -STATIC RAM APPLICATION-

Tetsuya IIZUKA and Takayasu SAKURAI

Semiconductor Device Engineering Laboratory
Toshiba Corporation
1-Komukai Toshiba, Saiwai-ku
Kawasaki 210 Japan
81-44-511-2111 ex 2676

Introduction

Since 1978(1), alpha-particle induced failures have been studied intensively on dynamic memories, which are susceptible to alpha-particle generated charge since they store data in terms of charge. Static RAM cell with active loads or relatively low resistive loads are immune to alpha-particle induced charges. However, high density static cells with very high resistive loads are also susceptible to alpha-particle injection(2). Because of smaller static cell capacitance, it may well be weaker than dynamic cells.

The objectives of this paper are to investigate the soft error rate (SER) reduction of very high resistive load static cells by CR-decoupling of gate electrodes from junctions exposed to alpha-particle generated charge.

Alpha-Particle Generated Current

According to Hsieh et al.(3), drift component of alpha-particle induced current flows within less than one nanosecond by the funneling mechanism, creating a huge current pulse height, and after that, the rest of alpha-particle generated charges are collected by diffusion. The diffusion current is relatively low, and a large fraction is expected to be collected to adjacent n^+ diffusion region and, in the case of p-well structured cell, to n-type substrate. The cell layout technique(2) is thus effective to immunize against diffusion collected charges. On the other hand, because of very fast charge collection by the funneling mechanism, the drift current has seriously high pulse height, several orders of magnitude higher than resistive load supplied current. The funneling current is considered to be localized to the alpha-particle incident point. Thus the layout technique is not effective to prevent the drift current induced soft errors.

CR Isolated Cell

To improve the immunity to drift component of alpha-particle generated current, we propose the CR decoupling scheme that a CR time constant isolates the major storage charge from the drift collected charge at drain junctions. The scheme is also applicable to dynamic cells, as will be reported elsewhere. In this paper, however, we concentrate on the application for static cells with high resistive loads. A schematic drawing of the CR isolated static cell is illustrated in Fig. 1. Resistors, R_g, are inserted between drain diffusion regions and polysilicon gate electrodes. The resistor can be either distributed gate resistance or lumped one between gate and drain regions. Although the charge, Q_j, at the "H"-state drain region is easily lost by alpha-particle generated charge, Q_a, the charge, Q_g, stored at gate electrode can be protected from the drift component, if the time constant, C_gR_g, is sufficiently large.

If the drift collected alpha-particle charge, Q_a, is smaller than Q_j+Q_g, the cell data is not broken, and the final "H"-state memory node potential, V_{Hf}, is given as

$$V_{Hf} >= \frac{Q_j+Q_g-Q_a}{C_j+C_g}$$

where the current supplied by resistive load, R_L, is neglected.

When $Q_a>=Q_j+Q_g$, which is usually the case for high density static RAMs, the cell node potential V_{Hf} is dependent on R_g. In Fig.2, a simulated V_{Hf} in the case of standby mode is shown as a function of R_g for various values of C_j with fixed C_g=10fF. Higher V_{Hf} is obtained for smaller C_j owing to the larger current compensation by the diffusion current injected at the forward biassed drain junction.

Assuming that the failure condition is $V_{Hf}<0$, a minimum alpha-particle generated current to cause soft error, I_{a-min}, is obtained by simulation as a function of R_g as shown in Fig. 3. For R_g's larger than critical resistance, R_{g-crit}, the minimum current, I_{a-min}, is infinitely large, that is, the cell is free from soft error caused by alpha-particle injection. The critical resistance, R_{g-crit}, is approximated by

$$R_{g-crit}=\frac{t_a}{C_g*\ln\{(1+V_H/V_F)/(1+C_j/C_g)\}}$$

where V_H is the initial "H"-state node potential, V_F the n^+p junction forward bias and t_a the alpha-particle induced funneling current pulse width.

When the cell is selected, i.e. the word line voltage is raised to Vcc, cells with larger C_j are saved from the soft error with smaller resistance R_g, as shown in Fig. 4. This is due to the fact that a large fraction of the alpha-particle induced drift current is compensated by selection-gate supplied current.

Write Time Requirement

It is clear that the cell with larger R_g has wider margin against the alpha-particle induced failure. However, the maximum value of R_g

is limited by the time required for write operation. In Fig. 5, simulated write delay time, a delay time from bit line signal to memory cell flip, is plotted against R_g. It is seen that the write delay time is determined by C_g, R_g and MOS transistor resistance, and that the delay is short enough for large storage bit capacity MOS RAMs as far as R_g is smaller than 200 kilo-ohm. Therefore, referring to Figs.3 to 5, R_g has a wide range of solution to realize a static cell immune to drift collected alpha-particle generated carriers without sacrificing write operations.

Discussions

After the termination of funneling, injected carriers at the forward biassed drain junctions to compensate drift collection are expected to diffuse out to adjacent n^+-regions and also back to the same drain region together with the rest of alpha-particle generated charge. The current caused by these carriers has to be leveled down by the cell layout technique and well-structures to achieve soft error free resistive load cell.

References

(1) T.C. May and M. H. Woods, "A New Physical Mechanism for Soft Errors in Dynamic Memories", IEEE Trans. on Elec. Dev., pp2-9; Jan., 1979.

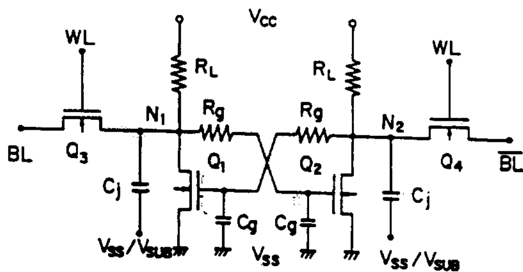

Fig.1. CR isolated static cell with resistive loads.

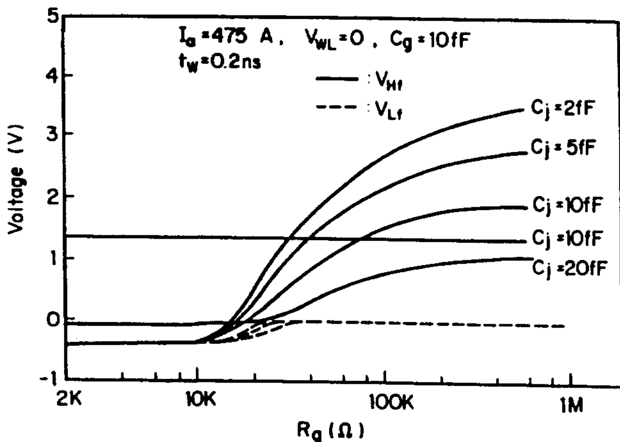

Fig.2. Calculated "H"-state memory node voltage after the drift collection of alpha-particle generated charge in standby mode.

(2) K. Anami, M. Yashimoto, H. Shinohara, Y. Hirata, H. Harada and T. Nakano, "A 35ns 16K NMOS Static RAM", 1982 ISSCC Dig. of Technical Papers, pp250-251, Feb., 1982.

(3) C. M. Hsieh, P. C. Murley and R. R. O'Brien, "Dynamics of Charge Collection for Alpha-Particle Tracks in Integrated Circuits", Proc. of IEEE Int. Reliability Physics Symposium, pp38-42; April 7, 1981.

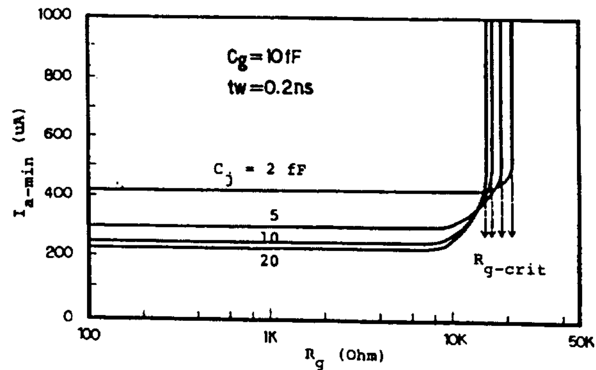

Fig.3. Minimum alpha-particle induced funneling current to cause memory cell flip, obtained by simulation.

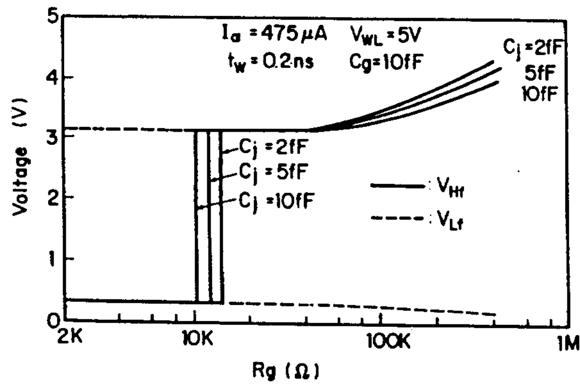

Fig.4. Calculated "H"-state memory node voltage after the drift collection of alpha-particle generated charge in read mode.

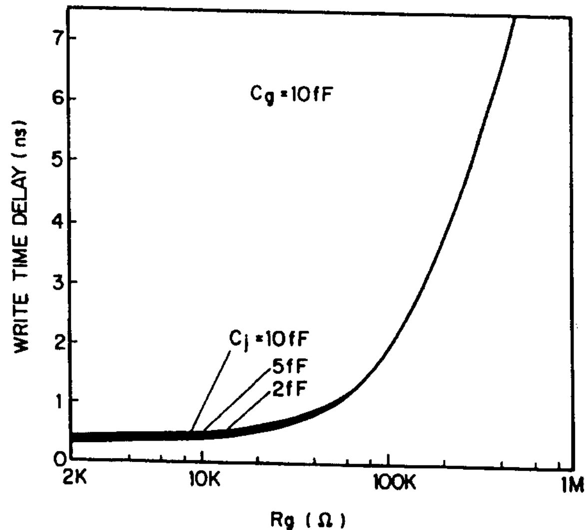

Fig.5. Simulated write delay time vs. R_g.