

# Through Silicon Capacitive Coupling (TSCC) Interface for 3D Stacked Dies

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**Abstract**

A Through Silicon Capacitive Coupling (TSCC) interface enabling face-to-back capacitive coupling data transfer for 3D stacked dies is proposed. TSCC has three features, (1) it allows stacking more than three chips, (2) it enables easy access to the bonding pads for DC power supplies, and (3) it enables the capacitive coupling pads to be used as bonding pads. TSCC channel models are assumed and design guidelines are given for transceiver design. A transceiver designed and fabricated in 0.18 $\mu\text{m}$  CMOS successfully communicates through a 400 $\mu\text{m}$  silicon substrate at 200Mbps. It is also shown that thinning the chip will reduce the area overhead of the TSCC pad.

**1. Introduction**

Proximity communication using capacitive coupling and inductive coupling is a low power and low cost alternative to TSV's. There are some problems which hinder the adoption of these interfaces.

Capacitive coupling channels have only been able to be integrated in a face-to-face fashion [1-3]. Only two chips can be stacked, and bonding wires to the chips is difficult to implement [2] as shown in Figure 1(a).

Inductive coupling channels enable the chips to be stacked in a face-to-back fashion [4]. This enables stacking more than 3 chips but the interface needs inductors. Since merging an inductor and a bonding pad is difficult, the interface cannot be shared with a normal bonding pad, requiring it to be used solely for the purpose of communication between 3D stacked dies.

The target of this work is a capacitive coupling interface which is capable of face-to-back communication. This enables (1) more than 3 tiers of chips to be stacked, (2) easy access to bonding pads for DC power, and (3) sharing of the bonding pad and capacitive coupling pad.

In this paper, a Through Silicon Capacitive Coupling (TSCC) interface which sends data through silicon substrate using capacitive coupling is proposed.

**2. Through Silicon Capacitive Coupling (TSCC)**

A conventional face-to-face capacitive coupling integration is shown in Figure 1 (a). Stacking more than two chips is impossible, and the bonding wire for DC power pins is difficult [2].

Figure 1 (b) shows the proposed face-to-back TSCC. The pads on the upper chip are facing up, so stacking more

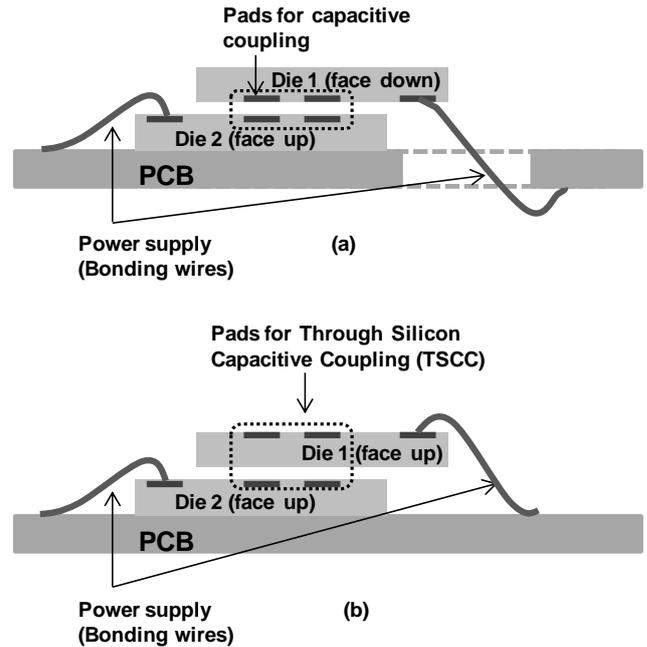


Figure 1(a) Conventional face-to-face, and (b) proposed face-to-back integration.

than three chips is possible, and bonding the DC power supplies is straightforward.

Figure 2 is the cross-section of the TSCC channel showing the underlying layers of the silicon substrate be-

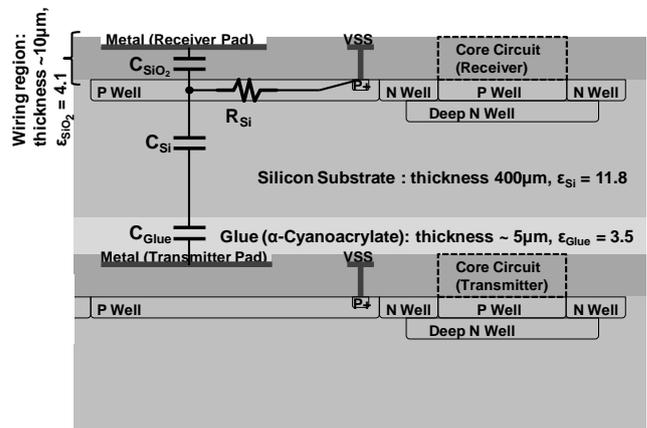


Figure 2 Cross-section of TSCC channel with assumed channel model.

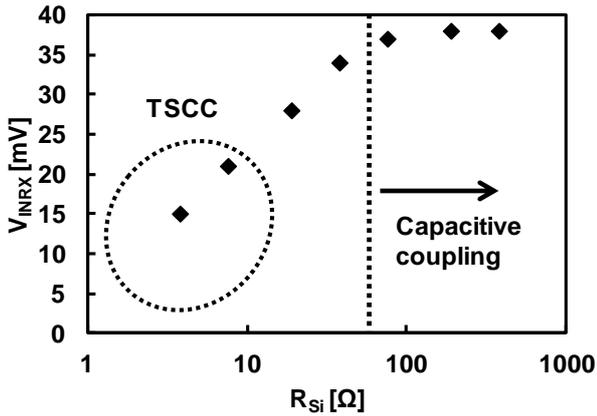


Figure 3 Simulated channel characteristics when pulse is sent from the transmitter pad to the receiver pad in Figure 2 under various  $R_{Si}$  values.

tween the transmitter pad and receiver pad. The silicon substrate is both a dielectric and a conductor. The channel model is approximated and also drawn in this figure.

Figure 3 shows the channel characteristics under various resistance values. The plateau at higher resistance values is determined by the coupling capacitance and parasitic capacitance as is the case with conventional capacitive coupling. The lower resistance region is where the proposed TSCC channel is used, so the factors determining

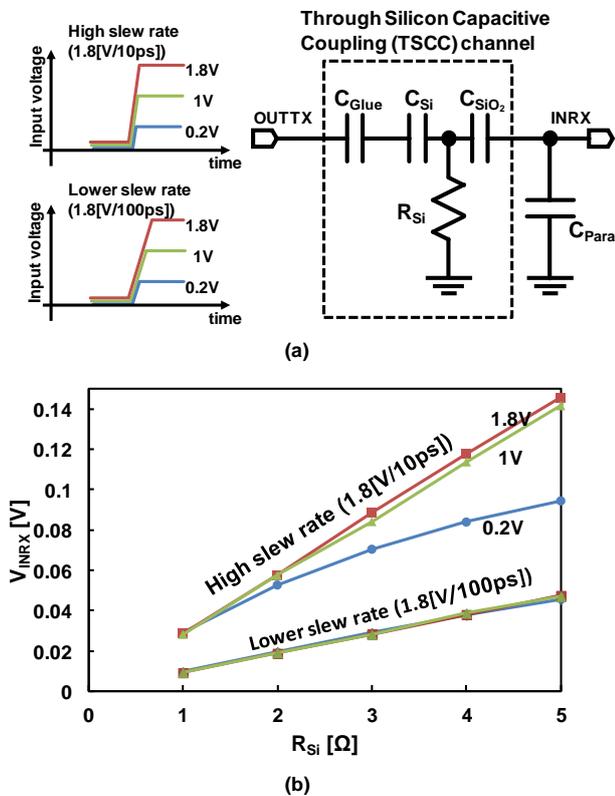


Figure 4(a) Simplified model of TSCC channel, and (b) simulated channel characteristics with different input voltages and slew rates.

this slope should be determined.

To clarify the determining factors of the channel characteristics in the lower resistance region, the channel is simulated with inputs with two groups of input waveforms, one with a high slew rate and another with a lower slew rate. Figure 4(a) shows the simplified simulated model and figure 4(b) shows the simulated effect of  $R_{Si}$  on the amplitude of the receiver input. This shows that the output voltage of the transmitter does not have significant impact on the channel, but the slew rate and resistance value of the channel determines the input voltage of the receiver circuit. Therefore sizing the transmitter circuit is very important for TSCC unlike conventional capacitive coupling, while the signal amplitude itself has little impact on the input voltage.

### 3. Circuit Design

Figure 5 shows the TSCC transceiver circuit. The transmitter is a CMOS buffer to drive the transmitter pad. The receiver which is slightly altered from [5] but has a stronger transmission gate to minimize the offset, amplifies the input pulse with a CMOS inverter amplifier and stores the data with a CMOS latch. The receiver circuit can be divided into four parts; the first part is a low noise amplifier and replica bias circuit biasing the input at the logical threshold voltage of the following inverter (Inv 2). This portion determines the maximum operational frequency of the overall circuit. Inverter 2 is the second part. This inverter amplifies the signal and decouples the latch in the following part from the bias voltage of the first part. This part, if too weak, cannot change the data written in the latch while if too strong, will overwrite the data latched regardless of the previous data, with the DC offset mismatch. The third part, which consists of Inv 3 and Inv 4, is the latch. The input of the smaller feedback inverter (Inv 4) and the Inv 2 hold the input voltage of the main inverter (Inv 3) to a voltage either higher or lower than the logical threshold of the Inv 3. If the input of the main inverter crosses the logical threshold, the feedback inverter will hold the voltage. The final part is Inv 5, which brings the signal swing back to rail-to-rail. Detailed design optimization of this circuit will be discussed here on since the input voltages of TSCC circuits are small due to the attenuation by the conductance of silicon.

All the main inverters in this architecture are used around their logic threshold and any differences in the logic

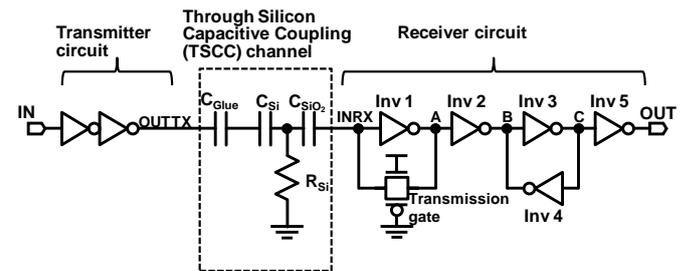


Figure 5 Schematics of TSCC transmitter and receiver circuits. Note the names of the nodes and inverters.

threshold between the inverters will negatively affect the sensitivity of the circuit. The P-N ratio of the inverter is determined first. When

$W_{PMOS} : W_{NMOS} = \mu_{NMOS} : \mu_{PMOS}$ , where  $W_{PMOS}$  and  $W_{NMOS}$  denote the width of the PMOS and NMOS transistors,  $\mu_{NMOS}$  and  $\mu_{PMOS}$  denote the mobility of NMOS and PMOS, the logic threshold becomes  $1/2V_{DD}$  and both the high pulses and the low pulses of the input are amplified symmetrically, leading to low jitter and high sensitivity. On the other hand, when

$W_{PMOS} : W_{NMOS} = \sqrt{\mu_{NMOS}} : \sqrt{\mu_{PMOS}}$ , the RC delay of the circuit is minimized, leading to maximum operational frequency. In this design, a PN ratio of 2:1 is used, which is in-between these two cases. Next the sizing of each inverter is discussed.

Inverter 5 simply recovers the output of the latch to rail-to-rail swing, so a standard cell size inverter (x1 inverter) is used since it does not need large gain or need to have small WID (WithIn Die) variation.

Inverter 3 also does not need to be large since it is only driving inverters 4 and 5, so a standard cell size inverter is large enough gain wise, but since the overall circuit is very sensitive to the mismatch of the logical threshold of this inverter, a x4 size inverter is selected for this design.

For inverter 5 to be “high”, the input of inverter 3 must be smaller than a certain voltage. This voltage can be determined by drawing a butterfly curve of inverter 3 and 5 as shown in figure 6. The voltage division of the channel resistance of inverter 2 at  $1/2V_{DD}$  and inverter 4 fully turned on, must be smaller than this voltage, determining the minimum ratio of inverter 2 and 4. Inverter 4 is made as small as possible, since this determines the size of inverter 2. In this design, minimum size transistor widths with  $0.5\mu\text{m}$  length transistors are used to make it small while reducing WID variation.

The size of inverter 2 is constrained by another factor. The input signal must be amplified enough by inverters 1 and 2, to be able to change the data stored in the latch. Having equal gain in inverters 1 and 2 is the most energy efficient so the size of inverters 1 and 2 are designed to be

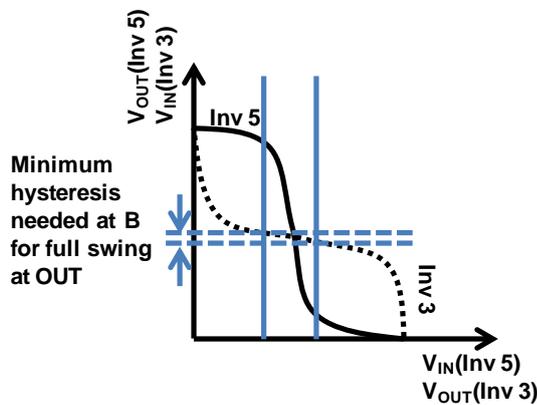


Figure 6 Illustration of butterfly curve of Inv 3 and Inv 5.

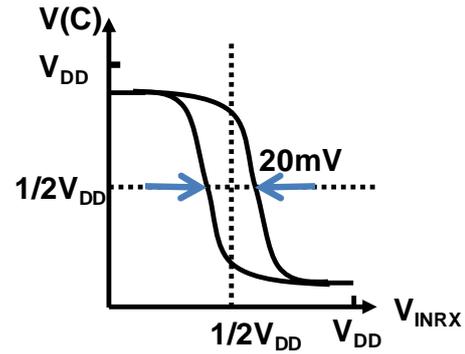


Figure 7 Illustration of the voltage at node C when input of whole receiver (INRX) is swept.

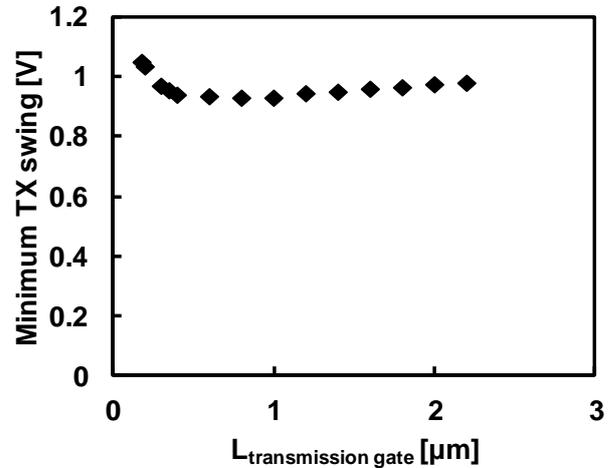


Figure 8 Simulated transmission gate gate length dependence on minimum detectable TX voltage swing.

the same size. The minimum input voltage that is detected must be determined by the thermal noise, ambient noise, voltage fluctuation, WID variation. In this case, 20mV is selected. With the size of inverter 4 fixed, and using the same sizes for inverter 1 and 2, monitoring node C while sweeping the input voltage of INRX of the whole circuit will reveal a hysteresis as shown in figure 7. The size of inverters 1 and 2 are determined so that the hysteresis seen at  $1/2V_{DD}$  is 20mV. In this design, a x4 size is selected.

Finally, the size of the transmission gate is determined. Since the transistors in the transmission gate are turned on, while inverter 1 only works around  $1/2V_{DD}$ , similar to the case of inverter 2 and 4, the width of the transistor is minimized, and the optimum gate length is searched for. When the transmission gate is too weak, the input will not return to  $1/2V_{DD}$  in time for the next signal, which will cause an offset which in turn will degrade the following signal pulse, but if the transmission gate is too strong, the signal will be attenuated. Figure 8 shows the simulation results where inputs of varying amplitude but with a fixed frequency are fed in to the TSCC. The gate length of the transmission gate is swept. This reveals the gate length with the highest sensitivity. Following these steps will

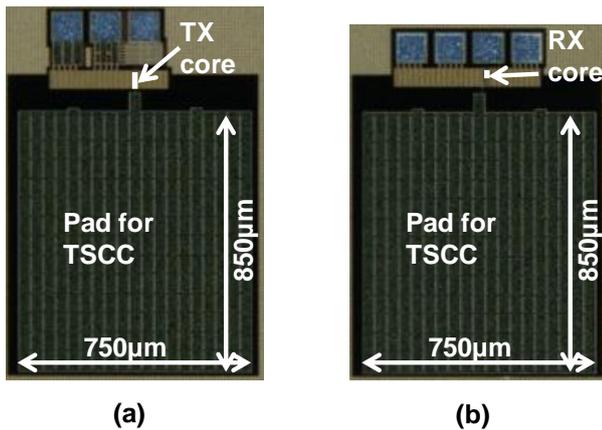


Figure 9 Chip micrograph of (a) transmitter, and (b) receiver with TSCC pads.

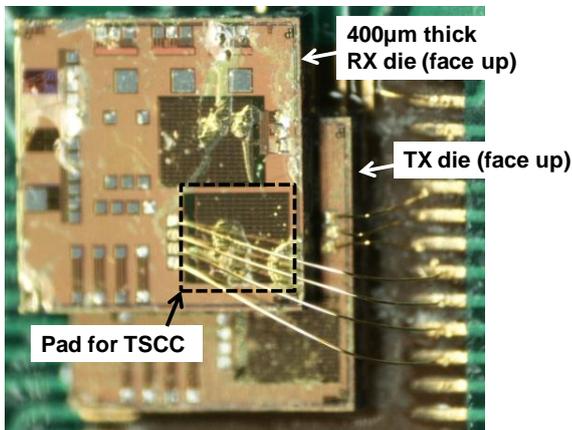


Figure 10 Photograph of 2-stacked dies for TSCC. lead to a 20mV input receivable TSCC circuit.

#### 4. Measurement Results

A TSCC transceiver chip is fabricated in  $0.18\mu\text{m}$  CMOS. The chip micrographs of the transmitter and receiver circuits are shown in Figure 9. The pad for TSCC is  $850\mu\text{m} \times 750\mu\text{m}$ . The core of the transmitter circuit is  $40\mu\text{m} \times 5\mu\text{m}$ , and the receiver circuit is  $20\mu\text{m} \times 5\mu\text{m}$ .

Figure 10 shows the stacked transmitter die and receiver die. The bottom die is the transmitter facing up, and the top die is the receiver which is also facing up. To enable TSCC, both transmitter and receiver circuits are in a deep n-well to make the silicon substrate floating and to keep the substrate contacts far away from the receiver pad so that the substrate resistance is high enough. The thickness of the receiver chip, which is equal to the communication distance, is  $400\mu\text{m}$ . This means that the coupling capacitance ( $C_c$ ) of the TSCC interface is  $160\text{fF}$ .

Figure 11 shows the measured input and output data waveforms. A  $2^7-1$  PRBS data is sent at 200Mbps. Correct data reception over the TSCC channel is confirmed.

Figure 12 shows calculated dependence of the pad area on the distance of TSCC at  $C_c$  of  $160\text{fF}$ . Since this is a feasibility study,  $850\mu\text{m} \times 750\mu\text{m}$  pads are used to communicate through a  $400\mu\text{m}$  thick substrate. To keep the am-

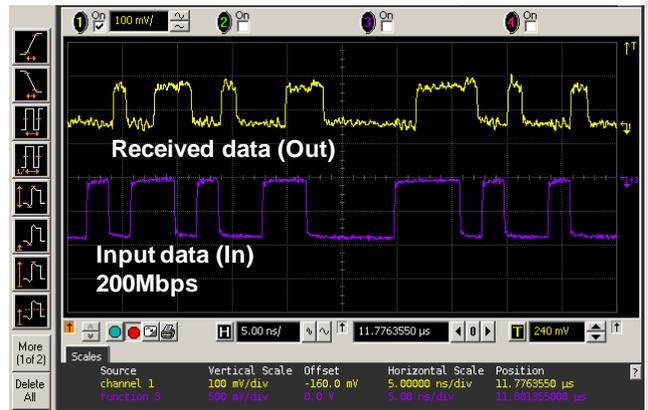


Figure 11 Measured input (bottom) and output (top) waveforms at 200Mbps.

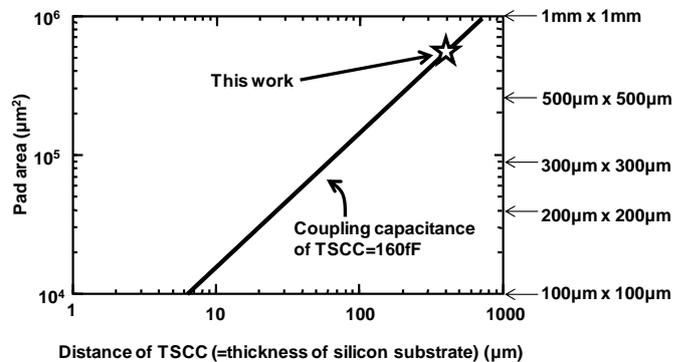


Figure 12 Calculated dependence of pad area on distance of TSCC when coupling capacitance of pads is  $160\text{fF}$ .

plitude of the received signal constant, if the substrate were to be thinned to  $50\mu\text{m}$ , the TSCC pad will be  $280\mu\text{m} \times 280\mu\text{m}$ . When thinned to  $10\mu\text{m}$ , the TSCC pad will be  $125\mu\text{m} \times 125\mu\text{m}$ , so the more the substrate is thinned, the more the area overhead of the TSCC pad is reduced.

#### 5. Conclusions

A Through Silicon Capacitive Coupling (TSCC) interface enabling face-to-back capacitive coupling data transfer for 3D stacked dies is proposed. This allows multiple tier stacking, easy access to bonding pads on all tiers, and sharing of pads between conventional bonding pads and TSCC. Channel characteristics of TSCC are modeled, revealing that the input slew rate of the transmitter is important in TSCC as opposed to capacitive coupling. Design optimization of the circuit for maximum sensitivity is shown. A transceiver designed in  $0.18\mu\text{m}$  CMOS successfully demonstrated communication through a  $400\mu\text{m}$  silicon substrate up to 200Mbps.

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