A 0.45-V Input On-Chip Gate Boosted (OGB) Buck Converter in 40-nm CMOS with More Than 90% Efficiency in Load Range from 2μW to 50μW

Xin Zhang[1], Po-Hung Chen[1], Yoshikatsu Ryu[2], Koichi Ishida[1], Yasuyuki Okuma[2], Kazunori Watanabe[2], Takayasu Sakurai[1], and Makoto Takamiya[1]
[1]University of Tokyo, Tokyo, Japan, [2]Semiconductor Technology Academic Research Center (STARC), Yokohama, Japan

Abstract

A 0.45-V input, 0.4-V output on-chip gate boosted (OGB) buck converter with clock gated digital PWM controller in 40-nm CMOS achieved the highest efficiency to date with the output power less than 40μW. A linear delay trimming by a logarithmic stress voltage (LSV) scheme to compensate for the die-to-die delay variations of a delay line in the PWM controller with good controllability is also proposed.

Introduction

Adaptive power supply voltage (V_{DD}) control is important for near-threshold logic circuits to achieve an energy efficient operation against PVT variations, because low V_{DD} circuits are very sensitive to the variations. In [1], a low dropout regulator (LDO) is used for the adaptive V_{DD} control. The LDO is, however, not suitable for the adaptive V_{DD} control, because the efficiency is limited to less than V_{OUT}/V_{IN}, where V_{OUT} is an output voltage and V_{IN} is an input voltage. To improve the efficiency, a 0.45-V V_{IN}, 0.4-V V_{OUT} buck converter with 2~50-μW output power (P_{OUT}) range is developed in this paper. The efficiency of the buck converter with such low V_{IN} and P_{OUT} is, however, normally low, because (1) the loss in power transistors increases due to low V_{IN} and (2) the controller power dominates the total power due to low P_{OUT}. Fig. 1 shows a calculated dependence of efficiency on quiescent power (= controller power). As the quiescent power increases, the efficiency decreases. For example, to achieve more than 90% efficiency at P_{OUT} of 2μW, the quiescent power should be less than 222nW. In order to achieve a high efficiency buck converter, this paper proposes (1) a gate boost by fully integrated switched-capacitor (SC) DC-DC converters to overdrive the power transistors in buck converter, (2) a low power clock gated 0.45-V digital PWM controller to improve the efficiency at low P_{OUT}, and (3) a linear delay trimming by a novel logarithmic stress voltage (LSV) scheme to compensate for the die-to-die delay variations of a delay line in the PWM controller with good controllability.

On-chip Gate Boosted (OGB) Buck Converter

Fig. 2 shows a block diagram of the proposed on-chip gate boosted (OGB) buck converter. Without OGB, driving voltages of the power transistors are low (=V_{IN}), thus the loss of the power transistors increases and the efficiency decreases. In order to reduce the on-resistance of the power transistors, a fully integrated $2V_{IN}$ (=double voltage) SC DC-DC converter for the nMOS power transistor (M_N) and a minus V_{IN} SC DC-DC converter for the pMOS power transistor (M_P) are developed to boost the supply voltages for the gate drivers. The PWM signal (CK_PWM) is boosted to "$-V_{IN}$ to V_{IN}" and "0V to $2V_{IN}$", for M_P and M_N, respectively. Fig. 3 shows a circuit schematic of a digital PWM controller and a clock gating controller. Instead of a conventional analog feedback control, a delay-line based digital PWM controller is newly developed for 0.45-V operation. A new clock gating technique is applied to shift registers (SR) in the PWM controller for power saving. Specifically, when V_{OUT} is higher than the high reference voltage ($V_{REF(H)}$) or lower than the low reference voltage ($V_{REF(L)}$), the clock signal (CK) is given to SR; when V_{OUT} is between $V_{REF(H)}$ and $V_{REF(L)}$, CK divided by 16 is given to SR, thereby reducing the controller power by 26%. Fig. 4 shows a schematic of a fully integrated $2V_{IN}$ SC DC-DC converter [2] employed in the proposed OGB buck converter.

Delay Line Trimming by LSV

In the digital PWM controller in Fig. 3, a delay-line without feedback control is used to minimize the controller power. Large die-to-die delay variations of the delay line at low V_{IN}, however, might fail the PWM operation. To compensate for the die-to-die process variations, a delay trimming by a charge injection is newly proposed, while the trimming to reduce a minimum operating voltage of an oscillator is previously proposed in [3]. Fig. 5 shows a schematic of the trimmed delay line. During the stress for the charge injection, V_{DD} is set to 1.1V. By applying a high n-well voltage as a stress voltage (V_{stress}), the absolute value of the threshold voltage of pMOS is raised to increase the delay. Fig. 6 shows a conventional linear stress voltage scheme and the proposed LSV scheme. Fig. 7 shows a measured stress time dependence of the delay of the trimmed delay lines. The conventional linear stress voltage scheme exponentially increases the delay, which means a poor controllability. In contrast, the proposed LSV linearly increases the delay, which means a good controllability. Fig. 8 shows a measured stress time dependence of the delay of the trimmed delay line and the retention characteristics for 8 dies. The target delay is set to five times of the initial delay to show the controllability of proposed LSV scheme. The linear delay trimming by LSV and the compensation of the die-to-die delay variations are successfully demonstrated. No significant retention degradation is observed.

Experimental Results

A die photo of the buck converter fabricated with a 40-nm CMOS is shown in Fig. 9. Table I shows a performance summary. The 140-nW quiescent power is less than the target 222nW in Fig. 1. Fig. 10 (a) shows measured waveforms of load regulation. Overshoot of 10mV and 8mV, and ripple voltage of 5mV are observed. Fig. 10 (b) shows a startup transition. At the beginning, when V_{OUT} is lower than $V_{REF(L)}$, the SR is clocked by CK of 20kHz. When V_{OUT} is between $V_{REF(L)}$ and $V_{REF(H)}$, the clock gating is activated thus the SR is clocked by (20/16)kHz, thereby reducing the power of the PWM controller. Fig. 11 shows the measured dependence of the efficiency on P_{OUT}. By using the proposed OGB, the efficiency is increased from 55% to 96% at P_{OUT} of 15μW. On the other hand, at P_{OUT} of 270nW, the efficiency is increased from 60% to 67% by the proposed clock gating of SR. At P_{OUT} range from 2μW to 50μW, the proposed buck converter achieves more than 90% efficiency (> ideal LDO efficiency=0.4V/ 0.45V=89%) with a peak value of 97% at 7μW. Fig. 12 shows the comparison with the published DC-DC converters [4-8]. The proposed buck converter achieved the highest efficiency to date with the output power less than 40μW. Moreover, the lowest input voltage is also achieved.

Acknowledgment

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References

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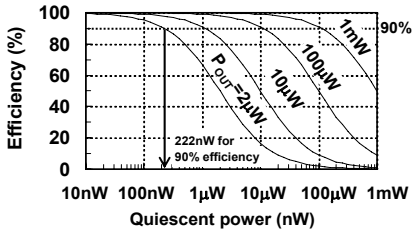


Fig. 1. Calculated dependence of efficiency on quiescent power.

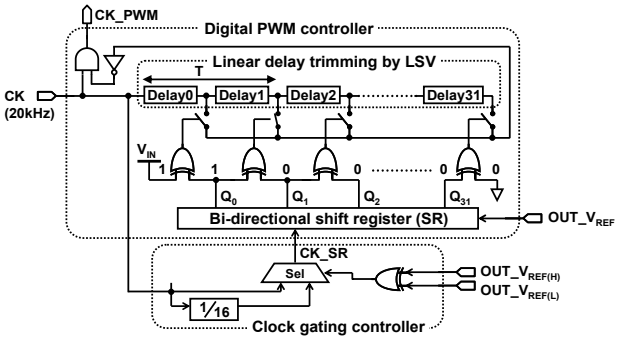


Fig. 3. Circuit schematic of digital PWM controller and clock gating controller.

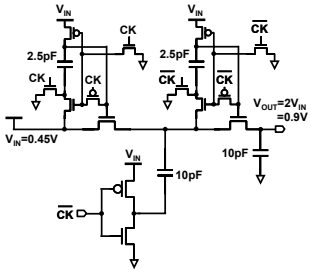


Fig. 4. Circuit schematic of $2V_{IN}$ (=double voltage) switched-capacitor (SC) DC-DC converter.

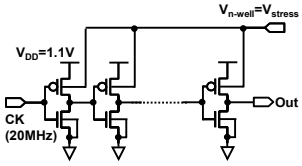


Fig. 5. Circuit schematic of trimmed delay line with charge injection.

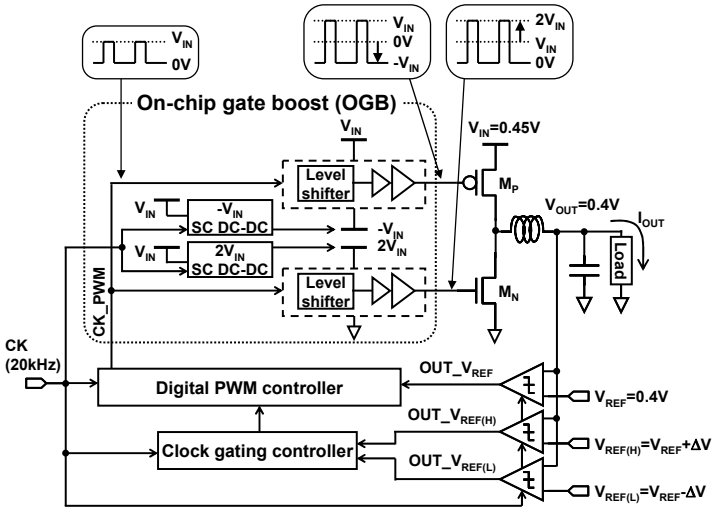


Fig. 2. Block diagram of proposed buck converter with on-chip gate boost and digital PWM controller.

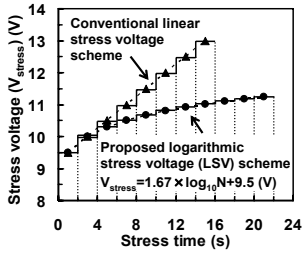


Fig. 6. Conventional linear stress voltage scheme and proposed logarithmic stress voltage (LSV) scheme.

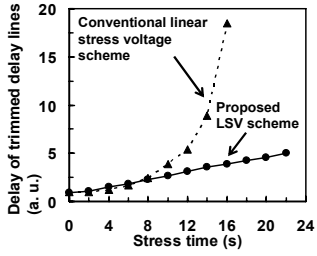


Fig. 7. Measured delay vs. stress time of conventional linear stress voltage scheme and proposed LSV scheme.

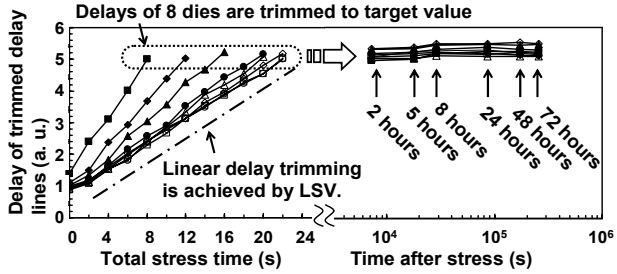


Fig. 8. Measured delay trimming by proposed LSV and retention characteristics for 8 dies.

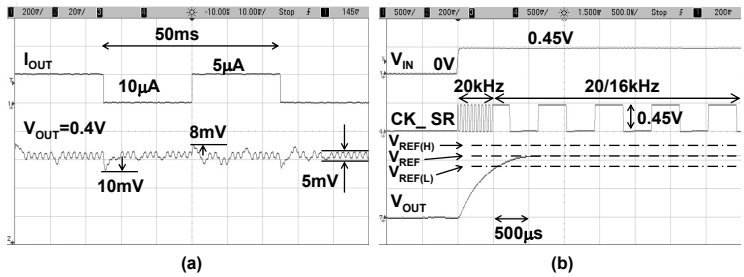


Fig. 10. Measured waveforms. (a) Load regulation. (b) Start up transition.

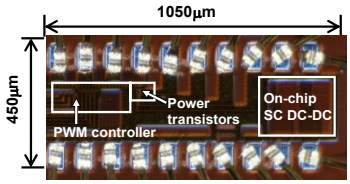


Fig. 9. Chip micrograph.

TABLE I Performance summary

Technology	**40-nm CMOS**
Input voltage	**0.45V**
Output voltage	**0.34V~0.44V**
Output power	**270nW~165μW**
Output ripple	**<5mV**
Max. efficiency	**97% at 7μW**
Quiescent power at I_{OUT}=0	**140nW**
Active area	**0.043 mm²**

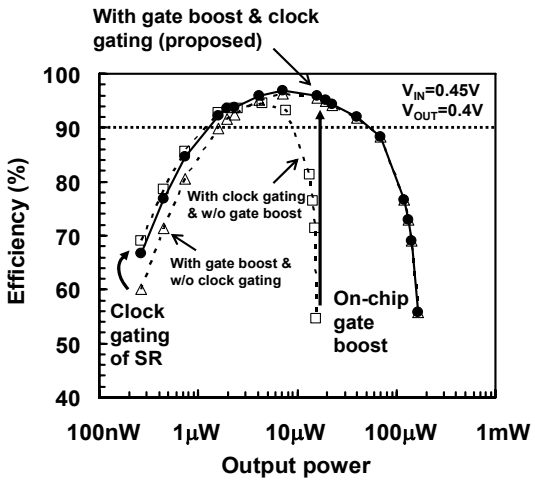
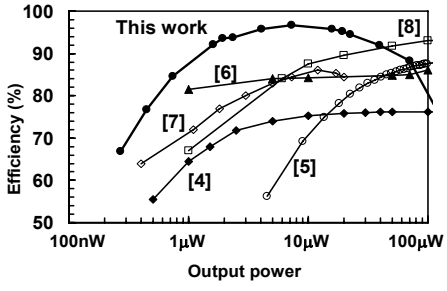


Fig. 11. Measured dependence of efficiency on output power with and without gate boost and clock gating of shift register.



Reference	[4] ISSCC 2008	[5] CICC 2010	[6] ISSCC 2007	[7] VLSI 2010	[8] VLSI 2011	This work
Type	Switched-capacitor	LDO	Buck	Buck	Buck	Buck
CMOS	65nm	65nm	65nm	130nm	250nm	40nm
Input voltage (V)	1.2	0.5	1.2	1.8	1.2	0.45
Output voltage (V)	0.5	0.45	0.5	0.575	1.0	0.4

Fig. 12. Comparison with published low voltage and low output power DC-DC converters.