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A 80-mV Input, Fast Startup Dual-Mode Boost Converter with Charge-Pumped Pulse Generator for Energy Harvesting

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***Abstract*—A low startup-voltage and fast startup dual-mode boost converter for energy harvesting applications is developed in 65-nm CMOS. Comparing with the previous work [6], the startup-time, the minimum startup voltage, and the program time are greatly improved. (1) A startup by the boost converter instead of a charge pump reduced the startup-time to 4.8ms which is 1/56 of [6] and the shortest to date. (2) The proposed sub-1nW charge-pumped pulse generator (CPPG) enabled the lowest startup voltage of 80mV to date without mechanical switch. (3) The proposed threshold-voltage-tuned oscillator with hot-carrier injection (HCI) for CPPG to compensate for the die-to-die process variations reduced the program time to 3min which is 1/20 of [6], thereby reducing the test cost.**

I. Introduction

Recently, the wireless sensor networks are widely employed in various applications including environmental monitoring, energy consumption monitoring, and bio-medical applications. The self-powered power management circuit applying energy harvester enables maintenance free sensors and extends their applications [1]-[2]. The thermoelectric generator can generate the output voltages in the range of 10mV/K to 50mV/K. For body-wearable applications, the output voltage is less than 100mV for temperature difference of 2K. The single-cell solar cell generates 500-600mV in the outdoor and 100-200mV in the dark office environment. The step-up DC-DC converter is required to boost the harvested energy to usable output because the harvested voltages are too low to power electronic devices.

The key challenge of the low-input step-up DC-DC converter for energy harvesting applications is to develop a startup mechanism, which kick-starts operation of the system from extremely low voltage. Until now, several startup techniques were reported [3]-[6]. In [3], it achieved the startup voltage of 35mV but an additional mechanical switch which is activated by motion vibration is required. In [4-5], the system is startup by a battery or an initial high voltage and the application is limited. In [6], a 95-mV startup voltage without using mechanical switch is realized by the capacitor pass-on scheme, as shown in Fig. 1, however, there still exists some problems. (1) It uses charge pump (CP) to charge the large output capacitor (C_{OUT}) and 262ms of startup time is required, (2) the leakage current shown in Fig. 1 limits the startup voltage to 95mV, and (3) the fixed-charge threshold voltage (V_{TH}) programming is applied but it takes 60min to adjust the minimum operation voltage (V_{DDMIN}) from 125mV to 82mV.

The 60-min programming time is too long, because the V_{TH} programming is performed at a pre-shipment test to compensate for the die-to-die variations and the long machine time of a tester raises a test cost.

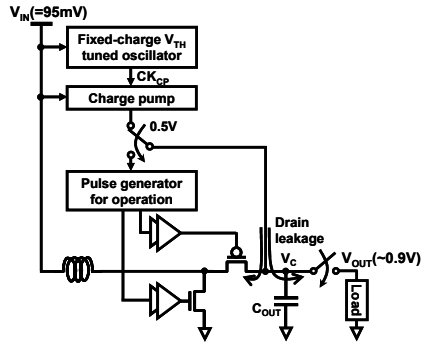

Fig. 1. Conventional boost converter [6]. Startup is achieved by charging C_{OUT} using charge pump.

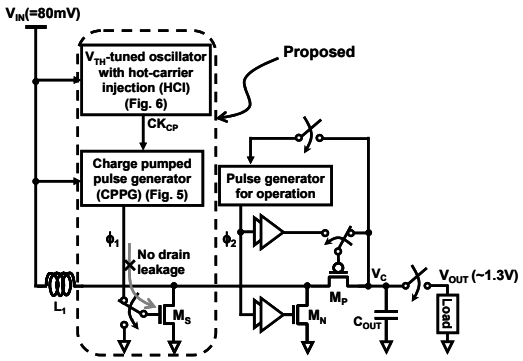

Fig. 2. Proposed dual-mode boost converter. Startup is achieved by charging C_{OUT} by boost converter with CPPG.

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In this paper, a 80-mV dual-mode boost converter is presented to solve these problems. The block diagram of the proposed dual-mode boost converter is shown in Fig. 2. The sub-1nW charge-pumped pulse generator (CPPG) is designed to activate the boost converter at startup mode. The lowest startup voltage of 80-mV with 56 times faster startup is therefore achieved. We also proposed a V_{TH}-tuned oscillator trimmed with hot-carrier injection (HCI) for CPPG to compensate for the die-to-die process variation. The V_{DDMIN} of the oscillator can be reduced from 130mV to 80mV within 3 minutes which is 20 times shorter than previous work [6].

This paper is organized as follows. The system architecture and the operation sequences of the proposed boost converter are described in Section II. Section III shows the circuit implementation of key building blocks in detail. The experimental results are shown in Section IV. Finally, conclusion will be drawn in Section V.

II. System Architecture

The proposed dual-mode boost converter consists of a boost core, a V_{TH}-tuned oscillator with HCI, a CPPG and a pulse generator for operation. The pulse generator is used to generate a pulse signal with fixed duty cycle and the output voltage is not regulated. The boost core includes power transistors M_P, M_N, and an additional power transistor M_S for startup. Comparing to the conventional approach [6], the proposed circuit startup by switching the transistor M_S instead of charging C_{OUT} by charge pump. In addition, the leakage current of the power transistors is eliminated because CPPG only drives the gate of M_S.

The startup sequences and waveforms of the proposed dual-mode boost converter are illustrated in Figs. 3 and 4. Fig. 3(a) shows the startup mode with low startup voltage and Fig. 3(b) shows the operation mode with high conversion efficiency. These modes can be automatically changed by detecting the capacitor voltage (V_C).

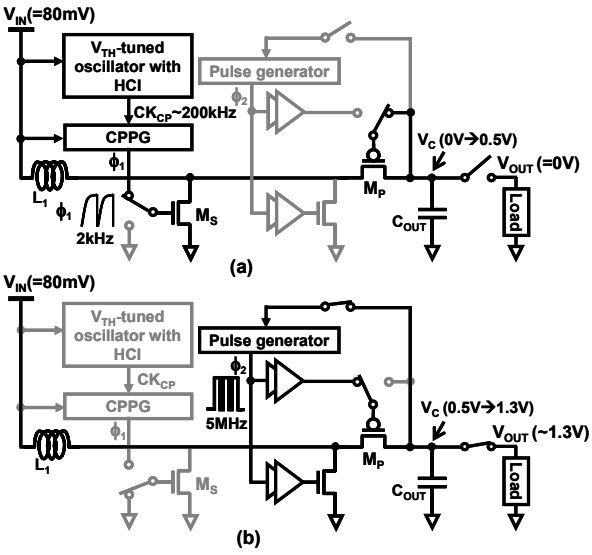

Fig. 3. Dual mode in the proposed boost converter (a) Startup-mode ($V_C \leq 0.5V$). (b) Operation mode ($V_C > 0.5V$) with high efficiency.

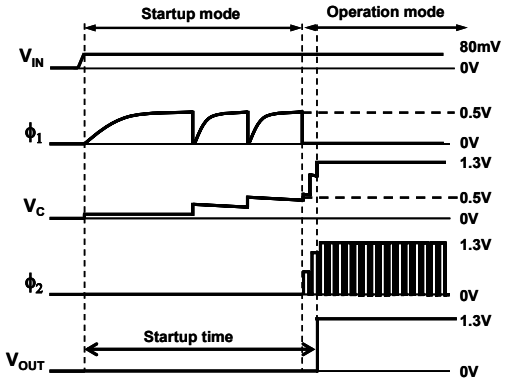

Fig. 4. Waveforms in startup sequences of dual-mode boost converter.

At the startup mode in Fig. 3(a), the V_{TH}-tuned oscillator with HCI provides the clock signal (CK_{CP}) to CPPG at the low input voltage (V_{IN}=80mV). CPPG converted V_{IN} to the high-amplitude pulse signal (ϕ_1) to activate the power transistor M_S. When ϕ_1 is high, M_S turns on and makes inductor current increases. When ϕ_1 changes from high to low, the current stored in inductor L_1 flow through the diode connected PMOS transistor M_P and charges C_{OUT}, as shown in Fig. 4.

When V_C is charged to the preset trigger voltage (0.5V), the boost converter changes the mode from startup mode to operation mode as shown in Fig. 3(b). V_C is detected by applying the voltage detector presented in [6]. At operation mode, the charge stored in C_{OUT} activates the pulse generator and the pulse generator starts driving the power transistors M_N and M_P to achieve high efficiency.

III. Circuit Implementation

A. Charge-Pumped Pulse Generator (CPPG)

The CPPG is the key building blocks in the proposed dual-mode boost converter. It converts the low V_{IN} to the high-amplitude pulse signal (ϕ_1) to activate the power transistor M_S exceeding the amplitude of trigger voltage (~0.5V). The proposed CPPG provides a solution for generating 0.5-V amplitude pulse signal with sub-1nW at low V_{IN} using CMOS process.

Fig. 5(a) shows the circuit schematic of the proposed CPPG. It includes a Dickson charge pump and a 0.5-V voltage detector (VD1) [6]. The trigger voltage of VD1 is determined by transistor size [6] and VD1 limits the output voltage of CPPG to be 0.5V. The charge pump is used to boost V_{IN}. Since the amplitude of CK_{CP} is 80mV, only 1nW output power can be extracted from the charge pump. The power consumption of the conventional CMOS ring oscillator is larger than 10nW and can not be used in this application. Therefore, the CPPG is proposed to generate the pulse signal with sub-1nW power consumption.

Fig. 5(b) shows the simulated waveform of the proposed CPPG. Initially, V_{CP} is smaller than the trigger voltage of VD1 and V_G provides low. The charge pump charges the node V_{CP} and ϕ_1. During the charging cycle, since all the transistors are turned-off, the power consumption is very small while V_{CP}

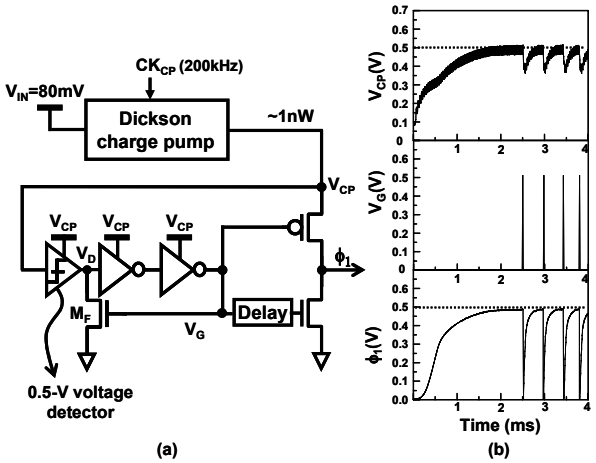

Fig. 5. Porposed sub-1nW charge-pumped pulse generator (CPPG). (a) Circuit schematic. (b) Simulated waveform.

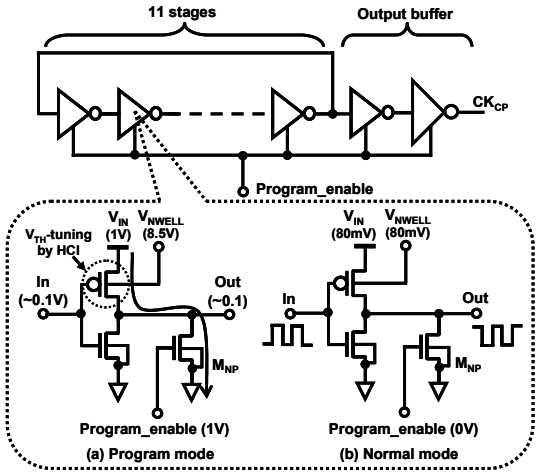

Fig. 6. Circuit schematic of proposed V_{TH}-tuned oscillator with hot-carrier-injection (HCI) for short program time. (a) Program mode. (b) Normal mode.

can still rise. As the V_{CP} is charged to the preset trigger voltage (0.5V) of VD1, V_G turns to high within 10μs and pulls down the voltage ϕ_1 to low. The delay cell is also added to guarantee that the ϕ_1 is discharged to low.

B. Threshold Voltage (V_{TH})-Tuned Oscillator with HCI

The V_{DDMIN} of an oscillator is usually limited by V_{TH} unbalance between NMOS and PMOS caused by process variation [7]. The within-die variation can be solved by increasing the transistor size. To make sure the circuit functions even under die-to-die process variation, we proposed a V_{TH}-tuned oscillator which trims the V_{TH} by HCI.

The detail circuit schematic is shown in Fig. 6. In the measured chips, since the V_{TH} of NMOS (V_{TN}) was higher than that of PMOS (V_{TP}). We illustrate PMOS programming only to simplify the schematic. Compared with the conventional approach [6] which uses AC pulse current for programming and requires 60min to adjust the V_{TH}, the proposed scheme in Fig. 6(a) provides DC current path for programming and the programming time can be reduced to 3min.

In PMOS post-fabrication programming by HCI, the high reverse body bias is applied to PMOS transistors (V_{NWELL}=8.5V) while the input voltage and the 1-V program enable signal are applied. The transistor M_{NP} is used to pull down the input and output voltages to 0V to draw a large DC current through the PMOS transistors. These bias conditions create hot carriers injection condition for PMOS transistors and increases $|V_{TP}|$.

After programming, the circuit is operating under normal mode as shown in Fig. 6(b) and only an 80-mV input voltage is applied. The injected holes are still fixed in the PMOS transistor and V_{TP} is now balanced with V_{TN} and V_{DDMIN} of the oscillator can be reduced.

IV. Experimental Results

The test chips were fabricated using 65-nm standard CMOS technology. The microphotograph of the proposed dual-mode boost converter is shown in Fig. 7 with active area of 0.25mm^2. Fig. 8 shows the measured dependences of V_{DDMIN} of the V_{TH}-tuned oscillator on program time using HCI. To verify V_{DDMIN} reduction, three test dies were measured. As can be seen, V_{DDMIN} can be reduced to 80mV with 3-minute program time. The V_{DDMIN} is improved by 45% within 10-minute program time. By using the proposed method, the test time can be reduced by 1/20 comparing to [6]. Therefore, the programming time and the test cost can be significantly reduced.

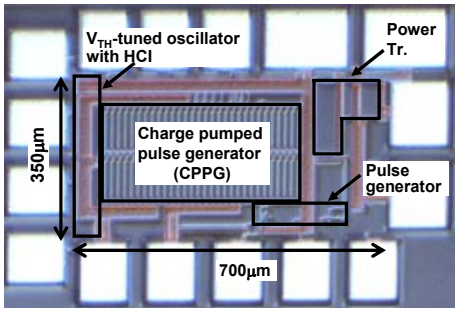

Fig. 7. Chip micrograph of dual-mode boost converter in 65-nm CMOS.

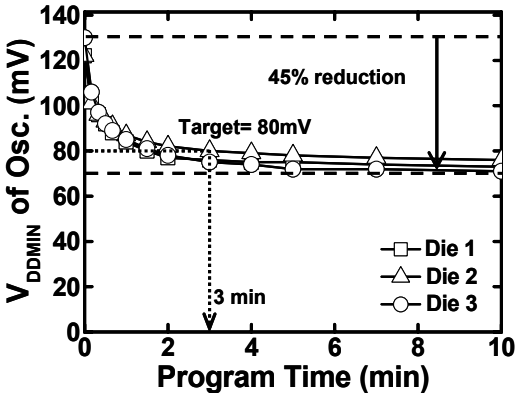

Fig. 8. Measured dependence of V_{DDMIN} of V_{TH}-tuned oscillator with HCI in Fig. 6(a) on program time for 3 dies.

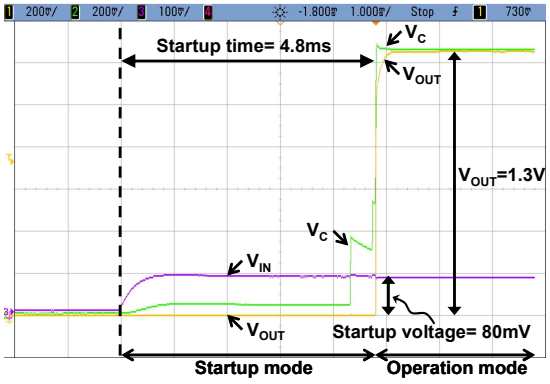

Fig. 9. Measured startup waveforms of proposed dual-mode boost converter.

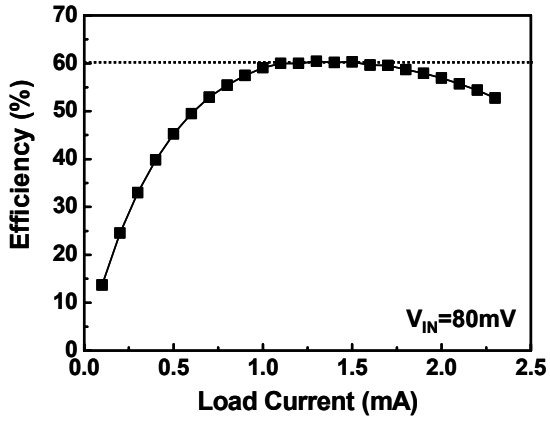

Fig. 10. Measured dependence of conversion efficiency on load current.

TABLE I. COMPARISON WITH PUBLISHED LOW-STARTUP VOLTAGE STEP-UP DC-DC CONVERTER

Ref	Startup			Peak Efficiency	Program time for Osc.	CMOS process
	Mechanism	*Min. Voltage*	*Startup time*			
[3]	Boost converter with mechanical switch	35mV	18ms	58%@ V_{IN}=50mV	–	350nm
[6]	Charge pump	95mV	262ms	72%@ V_{IN}=100mV	60min	65nm
[4]	External Voltage	650mV	N/A	75%@ V_{IN}=100mV	–	130nm
This work	Boost converter with CPPG	80mV	4.8ms	60%@ V_{IN}=80mV	3min	65nm

Fig. 9 shows measured startup waveforms of the proposed dual-mode boost converter with CPPG under 80mV input. The proposed dual-mode boost converter reduces the startup time to 4.8ms, which is 56 times shorter than [6]. Fig. 10 shows the measured dependence of conversion efficiency on different load current. The proposed circuit provides the maximum efficiency of 60% at 80mV input voltage.

The performance comparison with recently published low-startup voltage boost converters applying startup mechanism is shown in Table I. The proposed startup mechanism achieves the fastest startup time. Compared with the previous implementation by using CMOS process [6], it achieves 56 times shorter startup time. The proposed circuit also achieves the lowest startup voltage except for [3], which requires mechanical switch to assist startup. We also provide a solution for addressing die-to-die process variations using post-fabrication trimming with short program time. Therefore, the proposed circuit is practical for low-voltage energy scavenging applications.

V. CONCLUSIONS

A low startup-voltage and fast startup dual-mode boost converter is developed for energy harvesting applications. It provides the maximum conversion efficiency of 60% at 0.5mA load current with 80mV input voltage. Compared with the previous work [6], the proposed circuit greatly improves the startup-time, the minimum startup voltage, and the program time. The key features of the proposed work includes: (1) the startup time is reduced to 4.8ms which is 1/56 of [6] and is the shortest to date, (2) the lowest startup voltage of 80mV without using mechanical switch is achieved, and (3) the proposed V_{TH}-tuned oscillator with HCI to compensate for the die-to-die process variation reduced the program time to 3min which is 1/20 of [6], thereby reducing the test cost.

ACKNOWLEDGMENT

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