315MHz Energy-Efficient Injection-Locked OOK Transmitter and 8.4μW Power-Gated Receiver Front-End for Wireless Ad Hoc Network in 40nm CMOS

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Abstract

A 315MHz injection-locked OOK transmitter and a power-gated receiver front-end for wireless ad hoc network are developed in 40nm CMOS. The developed injection-locked frequency multiplier for carrier generation by edge combing achieves 11μW power consumption at 315MHz. The proposed power-gated low noise amplifier with current second-reuse technique achieves the lowest power consumption of 8.4μW with 7.9dB noise figure and 20.5dB gain in state-of-the-art designs.

Introduction

An ad hoc wireless sensor network refers to a group of spatially distributed sensors, or nodes, linked by a wireless medium to report on the physical world. Sensor nodes are usually powered either by batteries or through energy harvesting and thus each of the nodes should be implemented at a minimal power level.

Fig.1 shows the block diagram of the proposed low-power transceiver for wireless sensor network. The transceiver operates in a single channel centered at 315 MHz and employs on-off keying (OOK) modulation. The receiver uses an envelope detection based architecture that eliminates the need for a local oscillator and therefore most of the power is consumed by the front-end low noise amplifier (LNA) and the carrier generator. In this work a power-gated LNA with current second-reuse technique and an injection-locked frequency multiplier (ILFM) by edge combining for carrier generation are proposed to minimize the power.

Power Gated Amplifier with Current Second-Reuse

To archive low noise figure and 50-Ω input match, a large current is required at the first stage of the front-end amplifier. Current reuse technique can halve the current by stacking NMOS and PMOS transistors as amplifying devices [1]. As shown in Fig. 2, this current can be further reduced to 1/3 by overlapping the NMOS and PMOS pairs. The outputs of the two overlapped MOS pairs are summed in the second low DC-current stage. Fig. 3 shows the circuit implementation of the front-end shunt-feedback LNA with the proposed current second-reuse technique. Shunt feedback topology can not only prevent amplitude distortion and self-bias at the first stage but also eliminate the bias voltage generator for the second stage. The width of the overlapped transistors in the first stage is half of the top and the bottom transistors so the DC voltages at the overlapped points are \( V_{DD}/3 \) and \( 2V_{DD}/3 \) respectively which can be used as voltage bias for the second summation stage.

Power gating is an effective low-power design technique which originally stems from logic circuits where a circuit block is cut off from voltage supply when the block is not switching. In [2] power gating is introduced to the design of front-end LNA for pulse receiver. To keep the DC bias point when the amplifier is cut off, a replica of the amplifier, called bias keeper is used which dominates the power consumption of the receiver [2]. This bias keeper can be eliminated by two \( \Phi_{NG} \) controlled capacitors in Fig.3. During start-up, the voltage of the two capacitors is charged to \( V_{DD}/3 \) and \( 2V_{DD}/3 \) respectively. When the amplifier is cut off, DC bias voltage is held on the capacitors dynamically. As shown in Fig.4, this technique can also be applied to the mixer design to enable fast modulation and thus high energy efficiency.

Injection-Locked Frequency Multiplier

Principle of conventional injection-locked frequency multiplier is shown in Fig.5 (a) [3]. Assuming that the natural running frequency of the oscillator is very close to the \( N \)th harmonic of the reference, the oscillator will lock to that harmonic by injecting a stream of current pulses to the oscillator. Problems of conventional ILFM are narrow locking range and high power consumption. Without off-line tuning \( V_{tune} \), the locking range of an 8x 315MHz ILFM in this way is less than 1MHz. The 9.7ns settling time enables fast modulation in transmitter and fast power-gating in receiver. As shown in Fig.11, the measured power consumption of the LNA is reduced linearly with the power-gating duty and thereby achieves 8.4μW at 3.12% duty. The frequency multiplier spectrum and waveforms are shown in Fig.12. The measured power consumption and locking range of the frequency multiplier at \( f_{DD}/2 \) is 11μW and 5MHz respectively. Table I and Table II show the comparisons with state-of-the-art transmitter and receiver front-end LNA. The proposed power-gated LNA with the current second-reuse technique achieves the lowest power consumption of 8.4μW with 7.9dB noise figure and 20.5dB gain.

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References

Fig. 1. Injection-locked OOK transmitter and power-gated receiver.  
Fig. 2. Shunt-feedback LNA. (a) Typical. (b) Current reused. (c) Current second-reused.

Fig. 3. Proposed power-gated receiver front-end.  
Fig. 4. Proposed fast-settling OOK transmitter.  
Fig. 5. ILFM. (a) Pulse injection. (b) Edge combining.

Fig. 6. Circuit implementation of proposed ILFM.  
Fig. 7. Chip micrographs. (a) LNA. (b) ILFM.  
Fig. 8. Measured LNA noise figure and gain.

Fig. 9. Measured transmitter waveforms.  
Fig. 10. Measured LNA waveforms with 3.12% duty.  
Fig. 11. Measured LNA power dependency on duty.

Fig. 12. Measured ILFM spectrum and waveforms.

Table I. TX performance summary.  
Table II. LNA performance summary and comparison.

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