A Closed-form Expression for Estimating Minimum Operating Voltage ($V_{DDmin}$) of CMOS Logic Gates
Hiroshi Fuketa¹, Satoshi Iida¹, Tadashi Yasufuku¹, Makoto Takamiya¹, Masahiro Nomura², Hirofumi Shinohara², Takayasu Sakurai¹

¹Institute of Industrial Science, University of Tokyo, Japan
²Semiconductor Technology Academic Research Center (STARC), Japan

E-mail: {fuketa, sa-iida, tdsh, mtaka, tsakurai}@iis.u-tokyo.ac.jp, {nomura.masahiro, shinohara.hirofumi}@starc.or.jp

ABSTRACT
In this paper, a closed-form expression for estimating a minimum operating voltage ($V_{DDmin}$) of CMOS logic gates is proposed. $V_{DDmin}$ is defined as the minimum supply voltage at which circuits can operate correctly. $V_{DDmin}$ of combinational circuits can be written as a linear function of the square-root of logarithm of the number of logic gates and its slope is proportional to the standard deviation of the within-die variation in the threshold voltage difference between PMOS and NMOS transistors. The proposed expression is verified with Monte Carlo simulations using various gate chains. The verification reveals that $V_{DDmin}$ of inverter chains can be estimated within 11% error. The expression is also verified with silicon measurements in a 65nm CMOS process.

Categories and Subject Descriptors
B.7.0 [Integrated Circuits]: General

General Terms
Design, Measurement, Performance, Reliability

Keywords
Minimum operating voltage, subthreshold circuits, variations

1. INTRODUCTION
Scaling down the supply voltage below the threshold voltage ($V_{TH}$) is a promising approach for achieving ultra-low power circuits [1]. The reduction in the supply voltage, however, could cause functional errors, which is mainly caused by $V_{TH}$ variation. The supply voltage at which the first functional error occurs is defined as a minimum operating voltage ($V_{DDmin}$) in this paper.

According to [2], the ideal limit of $V_{DDmin}$ is estimated to 52mV. Actually, $V_{DDmin}$ is much higher than the ideal limit due to manufacturing variability. Niiyama et al. reported that $V_{DDmin}$ of ring oscillators rises as the number of logic gates increases [3]. Figure 1 shows $V_{DDmin}$ of an inverter chain as a function of the number of inverters in a 65nm CMOS process. While the difference of $V_{DDmin}$ between the nominal and worst process corners is induced by die-to-die $V_{TH}$ variation, the rise in $V_{DDmin}$ due to the increase in the number of logic gates is caused by within-die $V_{TH}$ variation. In mega gate scale circuits, the rise in $V_{DDmin}$ due to within-die $V_{TH}$ variation is comparable to that due
to die-to-die $V_{TH}$ variation. This suggests that the significant rise in $V_{DDmin}$ due to within-die $V_{TH}$ variation must be taken into account for the large-scale subthreshold circuit design.

A common way to obtain $V_{DDmin}$ with consideration for manufacturing variability is to exploit Monte Carlo simulations. However, the simulation time for larger circuits is extremely longer. Therefore, an alternative efficient method to estimate $V_{DDmin}$ is strongly required.

In this paper, a closed-form expression for estimating $V_{DDmin}$ of CMOS logic gates is proposed. Previous researches [2,4] mainly focused on techniques to decrease $V_{DDmin}$ by adjusting body-bias voltages, whereas a lot of attention to the modeling of $V_{DDmin}$ has not been paid. Although several prior works [5,6] modeled $V_{DDmin}$, the influence of within-die $V_{TH}$ variation has not been discussed well and hence it is not clear how $V_{DDmin}$ depends on the circuit size. This paper is the first work to model $V_{DDmin}$ quantitatively with consideration for both die-to-die and within-die $V_{TH}$ variations and to clearly reveal the dependence of $V_{DDmin}$ on the number of logic gates. The contribution of this paper is that $V_{DDmin}$ of combinational circuits can be easily estimated using the proposed model even in larger circuits.

The proposed model indicates that $V_{DDmin}$ of logic gates can be expressed as a linear function of the square-root of logarithm of the number of logic gates and its slope and intercept depend on within-die and die-to-die $V_{TH}$ variations, respectively. The proposed model is verified with Monte Carlo SPICE simulations using various gate chains in a 65nm and a 40nm CMOS process. This paper reveals that $V_{DDmin}$ of inverter chains can be well estimated by the model with less than 11% error. It is also shown that the proposed model can be applied to circuits fabricated in any manufacturing technologies, since the model is derived from subthreshold characteristics of a MOSFET.

Permission to make digital or hard copies of all or part of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage and that copies bear this notice and the full citation on the first page. To copy otherwise, to republish, to post on servers or to redistribute to lists, requires prior specific permission and/or a fee. DAC’11, June 5-10, 2011, San Diego, California, USA

© 2011 ACM 978-1-4503-0636-2/11/06...$10.00

984

Figure 1. $V_{DDmin}$ of inverter chain in 65nm CMOS process. $V_{DDmin}$ is calculated by closed-form expression proposed in this paper.
2. PROPOSED CLOSED-FORM EXPRESSION

In this section, a closed-form expression for \( V_{DDmin} \) of CMOS logic gates is proposed. In order to derive the closed-form model, an inverter chain is used. However, the model is not limited to an inverter and can be extended to other gates, such as NAND and NOR gates.

2.1 VDDmin of Inverter Chain

2.1.1 subthreshold characteristics of MOSFET

The I-V characteristic of a NMOS in subthreshold region is given by [5]

\[
I_n = \beta_n \cdot e^{\frac{V_{GS}}{U_T}} \cdot e^{\frac{V_{DS} - V_{th,n}}{U_T}} \left(1 - \frac{V_{DS}}{V_{th,n}}\right),
\]

where \( V_{GS} \) and \( V_{DS} \) are the gate-source and drain-source voltages, \( \beta_n \) is the subthreshold swing parameter, \( U_T \) is the thermal voltage, \( \eta_n \) is the DIBL (Drain Induced Barrier Lowering) coefficient, \( V_{th,n} \) is the threshold voltage at \( V_{DS} = 0 \) V, \( W_n \) and \( L_n \) are the gate width and length, and \( I_{0,n} \) is the technology dependent parameter.

When \( V_{DS} \) is much higher than \( U_T \), \((1 - e^{-V_{DS}/U_T})\) in (1) is close to 1, and hence (1) can be approximated to

\[
I_n = \beta_n \cdot e^{\frac{V_{GS}}{U_T}} \cdot e^{\frac{V_{DS} - V_{th,n}}{U_T}}
\]

(3)

On the other hand, when \( V_{DS} \) is much lower than \( U_T \), \((1 - e^{-V_{DS}/U_T})\) can be approximated to \( V_{DS}/U_T \) by truncating the Taylor series at the first order [5]. Thus, the subthreshold current can be expressed as

\[
I_n = \beta_n \cdot e^{\frac{V_{GS}}{U_T}} \cdot \frac{V_{DS}}{U_T} \quad \text{if} \quad V_{DS} \ll U_T.
\]

(4)

For a PMOS, \( \beta_p \), \( V_{Th,p} \), \( W_p \), \( L_p \), \( I_{0,p} \), \( \eta_p \), and \( \eta_p \) are substituted for \( \beta_n \), \( V_{th,n} \), \( W_n \), \( L_n \), \( I_{0,n} \), \( \eta_n \), and \( \eta_n \).

2.1.2 Logical threshold voltage

Figure 2 shows the voltage transfer characteristic of an inverter. When the input voltage is \( V_{IN} \) and the output voltage is \( V_{OUT} \), the currents of the NMOS and PMOS of the inverter are identical and from (1) can be expressed as

\[
I_n(V_{GS} = V_{IN}, V_{DS} = V_{OUT}) = I_p(V_{GS} = V_{IN}, V_{DS} = V_{OUT} - V_{DD}).
\]

(5)

Let \( V_{IL} \) and \( V_{IH} \) be input voltages where a unity gain is obtained and they are defined as the logical threshold voltages in this paper. \( V_{OUT}(V_{OL}) \) is output voltage when the input voltage is \( V_{IN}(V_{OH}) \).

When \( V_{IN} \) is lower than \( V_{IL} \), \( V_{OUT} \) is close to \( V_{DD} \), and hence the following equation is derived from (3), (4), and (5).

\[
\beta_n \cdot e^{\frac{V_{GS}}{U_T}} \cdot \frac{V_{DS}}{U_T} \beta_p \cdot e^{\frac{V_{GS}}{U_T}} \cdot e^{\frac{V_{DS} - V_{th,p}}{U_T}}
\]

(6)

where \( n=1/(1/\eta_p + 1/\eta_n)/2 \). When \( V_{IN} \) is \( V_{IL} \), the derivative of (7) with respect to \( V_{IN} \) is -1. Therefore,

\[
\beta_n \cdot e^{\frac{V_{GS}}{U_T}} \cdot \frac{V_{DS}}{U_T} \beta_p \cdot e^{\frac{V_{GS}}{U_T}} \cdot e^{\frac{V_{DS} - V_{th,p}}{U_T}} = -1.
\]

(7)

Consequently, \( V_{IL} \) and \( V_{OL} \) are obtained as follows.

\[
V_{il} = \frac{V_{DD}}{2} \left(1 - \frac{\eta_p}{\eta_n} \right) - \frac{1}{2} U_T \left(\ln\left(\frac{\beta_n}{\beta_p}\right) + \ln\left(\frac{2}{n}\right)\right),
\]

(9)

\[
V_{ol} = \frac{V_{DD}}{2} U_T.
\]

(10)

When \( V_{IN} \) is higher than \( V_{IH} \), \( V_{OUT} \) is close to the ground (\( V_{SS} \)). Thus, the following equation is derived from (3), (4), and (5).

\[
\beta_n \cdot e^{\frac{V_{GS}}{U_T}} \cdot \frac{V_{DS}}{U_T} \beta_p \cdot e^{\frac{V_{GS}}{U_T}} \cdot e^{\frac{V_{DS} - V_{th,p}}{U_T}}
\]

(11)

Since \( V_{OUT} \) is close to \( V_{SS} \), \( \exp(\eta_p V_{OUT}/n_p U_T) \) can be approximated to \( \exp(\eta_p V_{OUT}/n_p U_T) \). In the same manner as the abovementioned derivation for \( V_{IL} \), \( V_{IH} \) and \( V_{OL} \) can be written as

\[
V_{il} = \frac{V_{DD}}{2} \left(1 + \eta_n \right) + \frac{1}{2} U_T \left(\ln\left(\frac{\beta_p}{\beta_n}\right) + \ln\left(\frac{2}{n}\right)\right),
\]

(12)

\[
V_{ol} = \frac{1}{2} U_T.
\]

(13)

Figure 3 shows the comparison of the logical threshold voltages calculated by (9), (10), (12), and (13) with those obtained from (5) by numerical calculations. When \( n=1 \), the error between them is less than 4% as for \( V_{IL} \) and \( V_{IH} \), whereas the maximum error when \( n=2 \) reaches 20%. This is because the condition of the approximation in (4) is not satisfied when \( n \) is large. Since \( n \) is typically lower than 2, the logical threshold voltages can be calculated by (9), (10), (12), and (13) with moderate error.
2.1.3 Expression of \( V_{\text{DDmin}} \)

Next, the variations of the logical threshold voltages are examined. In this paper, only \( V_{\text{TH}} \) variation is considered. Random variables \( X_{\text{VTH}n} \) and \( X_{\text{VTH}p} \) are introduced to express within-die \( V_{\text{TH}} \) variation as follows.

\[
X_{\text{VTH},n} \sim N(0, \sigma_{\text{VTH,n}}^2), \quad X_{\text{VTH},p} \sim N(0, \sigma_{\text{VTH,p}}^2),
\]

(14)

where \( \sigma_n \) and \( \sigma_p \) are the standard deviations of within-die \( V_{\text{TH}} \) variations of PMOS and NMOS transistors, respectively.

Therefore, \( \beta_p \) and \( \beta_n \) in (2) can be written as

\[
\beta_p = I_{n,0} \frac{W}{L_p} e^{-\frac{X_{\text{VTH},n}}{nU_T}}, \quad \beta_n = I_{n,0} \frac{W}{L_n} e^{-\frac{X_{\text{VTH},p}}{nU_T}},
\]

(15)

(16)

From (9) and (12), \( V_{IL} \) and \( V_{IH} \) are given by

\[
V_{IL} = \frac{V_{TH,n}}{2} \left[ 1 - \frac{n}{n_p} \right] + \frac{n_p}{n} \left[ \ln \left( \frac{\beta_p}{\beta_n} \right) + \ln \left( \frac{2}{n} \right) \right] + X_{\text{VTH},n},
\]

(17)

\[
V_{IH} = \frac{V_{TH,p}}{2} \left[ 1 + \eta_p \right] + \frac{n}{n_p} \left[ \ln \left( \frac{\beta_p}{\beta_n} \right) + \ln \left( \frac{2}{n} \right) \right] + X_{\text{VTH},p},
\]

(18)

where

\[
X_{\text{VTH},n} = X_{\text{VTH},p} \sim N(0, \sigma_{\text{VTH}}^2),
\]

\[
\sigma_{\text{VTH}} = \sqrt{\sigma_n^2 + \sigma_p^2}.
\]

Equations (17) and (18) indicate that \( V_{IL} \) and \( V_{IH} \) are normally distributed due to within-die \( V_{\text{TH}} \) variation. Interestingly, on the other hand, \( V_{\text{OH}} \) in (10) and \( V_{\text{OL}} \) in (13) do not depend on \( V_{\text{TH}} \).

To investigate \( V_{\text{DDmin}} \), the conditions of failure are analyzed as depicted in Fig. 4. \( V_{\text{DDmin}} \) is equal to the minimum supply voltage at which the inverter B fails to receive signals from the inverter A. The conditions of the failure can be written as \( V_{\text{IL}} \) (of inverter B) > \( V_{\text{OH}} \) (of inverter A) and \( V_{\text{IH}} \) (of inverter B) < \( V_{\text{OL}} \) (of inverter A). Please note that we use these conditions instead of SNM (static noise margin) \[5,6\] since SNM is too strict for evaluating \( V_{\text{DDmin}} \) of gate chains.

Thus, the conditions where an inverter is functional are \( V_{IL} < V_{OH} \) and \( V_{IH} > V_{OL} \). From (10), (13), (17), and (18), the conditions can be written as

\[
\frac{n}{n_p} \left[ \ln \left( \frac{\beta_p}{\beta_n} \right) + \ln \left( \frac{2}{n} \right) \right] + X_{\text{VTH},n} + \frac{V_{TH,n}}{2} \left[ 1 - \frac{n}{n_p} \right] > \frac{V_{TH,n}}{2} \left[ 1 - \frac{n}{n_p} \right] + \frac{n_p}{n} \left[ \ln \left( \frac{\beta_p}{\beta_n} \right) + \ln \left( \frac{2}{n} \right) \right] + X_{\text{VTH},n},
\]

(21)

\[
\frac{n}{n_p} \left[ \ln \left( \frac{\beta_p}{\beta_n} \right) + \ln \left( \frac{2}{n} \right) \right] + X_{\text{VTH},p} + \frac{V_{TH,p}}{2} \left[ 1 + \eta_p \right] > \frac{V_{TH,p}}{2} \left[ 1 + \eta_p \right] + \frac{n}{n_p} \left[ \ln \left( \frac{\beta_p}{\beta_n} \right) + \ln \left( \frac{2}{n} \right) \right] + X_{\text{VTH},p},
\]

(22)

Thus, the following inequalities are obtained.

\[
g(V_{\text{DD}}) < X_{\text{VTH},n} < f(V_{\text{DD}}),
\]

(23)

\[
f(V_{\text{DD}}) = aV_{\text{DD}} + b - c, \quad g(V_{\text{DD}}) = -aV_{\text{DD}} + b + c,
\]

(24)

\[
a = l + \eta,
\]

(25)

\[
b = nU_j \ln \left( \frac{\beta_p}{\beta_n} \right) + \frac{n}{n_p} \left[ \ln \left( \frac{\beta_p}{\beta_n} \right) + \ln \left( \frac{2}{n} \right) \right] + X_{\text{VTH},n},
\]

(26)

\[
c = nU_j \left( 1 - \ln (2/n) \right),
\]

(27)

where \( n = n_p = n_n \) and \( \eta = \eta_p = \eta_n \).

Let \( P_{\text{INV}(V_{\text{DD}})} \) be the probability for an inverter to work without functional errors at \( V_{\text{DD}} \). \( P_{\text{INV}(V_{\text{DD}})} \) is the probability to meet the condition (23), and hence it can be expressed as

\[
P_{\text{INV}(V_{\text{DD}})} = P(g(V_{\text{DD}}) < X_{\text{VTH},n} < f(V_{\text{DD}})) = \Phi \left( \frac{f(V_{\text{DD}})}{\sigma_{\text{VTH,n}}} \right) - \Phi \left( \frac{g(V_{\text{DD}})}{\sigma_{\text{VTH,n}}} \right),
\]

(28)

where \( \Phi(x) \) is CDF (cumulative distribution function) of the Gaussian distribution.

Therefore, \( V_{\text{DDmin}} \) of an inverter chain is given by

\[
[P_{\text{INV}(V_{\text{DDmin}})}]^{N} = Y,
\]

(29)

where \( N \) is the number of inverters and \( Y \) is the probability that the inverter chain is functional at \( V_{\text{DDmin}} \). i.e. \( Y \) is the yield.

According to the Williams formula \[7\], \( \Phi(x) \) can be approximated to

\[
\Phi(x) = \left\{ \begin{array}{ll} 1 - \frac{1}{2} \left[ 1 - \exp \left( -\frac{-2x^2}{\pi} \right) \right]^{1/2} & (x \geq 0), \\ 1 - \frac{1}{2} \left[ 1 - \exp \left( -\frac{-2x^2}{\pi} \right) \right]^{1/2} & (x \leq 0). \end{array} \right.
\]

(30)

(31)
When \( \exp(-2x^2/\pi) \ll 1 \), the following approximation is given

\[
\Phi(x) = 1 - \frac{1}{4} \exp\left(-\frac{2x^2}{\pi}\right) \quad (x \geq 0),
\]
\[
\approx \frac{1}{4} \exp\left(-\frac{2x^2}{\pi}\right) \quad (x \leq 0).
\]

In the nominal condition, \( f(V_{dd}) > 0 \) and \( g(V_{dd}) < 0 \). Thus, the following equation is derived from (28), (32), and (33).

\[
P_{off}(V_{dd}) = 1 - \frac{1}{4} \exp\left(-\frac{2}{\pi}\left(f(V_{dd})\right)^2\right) + \exp\left(-\frac{2}{\pi}g(V_{dd})\right).
\]

When PMOS and NMOS transistors are perfectly balanced, i.e. \( b=0 \), \( f(V_{dd}) = -g(V_{dd}) \). Therefore, (29) can be written as

\[
[P_{on}(V_{dmin})]^N = \left[1 - \frac{1}{2} \exp\left(-\frac{2}{\pi}f(V_{dmin})\right)\right]^N = Y.
\]

Here, the following approximation is introduced.

\[
1 - \frac{1}{2} \exp\left(-\frac{2}{\pi}f(V_{dmin})\right) = 1 - \frac{N}{2} \exp\left(-\frac{2}{\pi}f(V_{dmin})\right). \quad (36)
\]

From (35) and (36), \( V_{dmin} \) can be expressed as

\[
V_{dmin} = \frac{\sigma_{pn}}{a} \sqrt{\frac{2}{\pi}} \ln\left(\frac{N}{2(1-\pi)}\right) + \frac{c}{a} \quad (37)
\]

Generally, PMOS and NMOS transistors are not completely balanced, and the unbalance is relatively large. In this case, \( P_{on}(V_{dd}) \) in (34) can be approximated to

\[
P_{on}(V_{dd}) = 1 - \frac{1}{4} \exp\left(-\frac{2}{\pi}f(V_{dmin})\right) \quad \text{if} \quad \beta_p > \beta_n,
\]
\[
P_{off}(V_{dd}) = 1 - \frac{1}{4} \exp\left(-\frac{2}{\pi}g(V_{dmin})\right) \quad \text{if} \quad \beta_p < \beta_n. \quad (39)
\]

By applying the same approximation as (36) to (29), \( V_{dmin} \) is derived as

\[
V_{dmin} = \frac{\sigma_{pn}}{a} \sqrt{\frac{2}{\pi}} \ln\left(\frac{N}{4(1-\pi)}\right) + \frac{c-b}{a} \quad \text{if} \quad \beta_p > \beta_n, \quad (40)
\]
\[
V_{dmin} = \frac{\sigma_{pn}}{a} \sqrt{\frac{2}{\pi}} \ln\left(\frac{N}{4(1-\pi)}\right) + \frac{c+b}{a} \quad \text{if} \quad \beta_p < \beta_n. \quad (41)
\]

The expression of \( V_{dmin} \) in (37), (40), and (41) indicates that 1) \( V_{dmin} \) is a function of the square-root of logarithm of the number of inverters \( N \), 2) the slope is proportional to \( \sigma_{pn} \), which is the standard deviation of the within-die \( V_{TH} \) difference variation defined in (20), 3) the balance of the strength of PMOS and NMOS transistors, which is expressed as the parameter \( b \) in (40) and (41), affects the intercept. The parameter \( b \) is fluctuated due to die-to-die \( V_{TH} \) variation.

Prior works [2,4] proposed the technique that makes the strength of PMOS and NMOS transistors well-balanced in order to attain ultra-low voltage operation. This technique is beneficial to reduce the parameter \( b \), whereas they have no effects on the slope in (40) and (41). This indicates that the rise in \( V_{dmin} \) caused by within-die \( V_{TH} \) variation become much larger as \( N \) increases and cannot be mitigated by the conventional technique, which could be a critical problem in large-scale circuits as shown in Fig. 1.

### 2.2 VDDmin of NAND and NOR Chains

The previous section has focused on the \( V_{dmin} \) of an inverter chain. The closed-form expression in (37), (40), and (41) can be extended to NAND and NOR gates by considering them equivalent inverters as shown in Fig. 5. While Alioto et al. only adjust the transistor strength \( \beta \) [5], this paper characterizes \( n \) and \( \eta \) in addition to \( \beta \). The logical threshold voltage can be calculated by applying these characterized parameters to (9), (10), (12), and (13).

In addition, \( \sigma_{pn} \) of the equivalent inverter is necessary to calculate \( V_{dmin} \). Figure 6 depicts the standard deviation of the variations in \( V_{il} \) and \( V_{ih} \) of an inverter, a two-input NAND2 gate, and a NOR2 gate obtained by SPICE Monte Carlo simulations (10,000 tries). It is assumed that the gate lengths and widths of transistors contained in the NAND2 and NOR2 gates are equal to those of the inverter. This figure indicates that the variations in \( V_{il} \) and \( V_{ih} \) of the NAND2 and NOR2 are nearly identical to those of the inverter. This is because one of stacked/paralleled transistors is always pulled-up to \( V_{dd} \) or pulled-down to \( V_{ss} \) and hence the influences of those transistors are relatively small. Therefore, the closed-form model can be applied to NAND and NOR gates with the characterized parameters and the same \( \sigma_{pn} \) as an inverter.
3. MODEL VERIFICATION

3.1 Simulation Setup

Various-stage gate chains up to 1001 stages are used for SPICE Monte Carlo simulations to obtain $V_{DD_{min}}$ as shown in Fig. 7. $V_{DD}$ is swept from 0 V. When $V_{DD}$ is lower than $V_{DD_{min}}$, $V_{OUT}$ at $V_{IN} = 0$ V is equal to $V_{OUT}$ at $V_{IN} = V_{DD}$. As the supply voltage increases, the difference between the output voltages at $V_{IN} = 0$ V and at $V_{IN} = V_{DD}$ becomes larger. In this paper, $V_{DD_{min}}$ is defined as the supply voltage at which the voltage difference reaches 50% of $V_{DD}$. 100 Monte Carlo simulations are performed with within-die $V_{TH}$ variation. Consequently, $V_{DD_{min}}$ distribution is obtained. In this paper, $V_{DD_{min}}$ of the circuit is defined as the median of the distribution, which means the yield is 50%.

3.2 Comparison of Model with Simulation

In this section, $V_{DD_{min}}$ calculated by the closed-form model in (37), (40) and (41) is compared with $V_{DD_{min}}$ obtained by the Monte Carlo SPICE simulations explained in Section 3.1. Figure 8 shows $V_{DD_{min}}$ of the inverter chain as a function of the number of stages $N$ and with various conditions of within-die $V_{TH}$ variation. $V_{DD_{min}}$ of the inverter chain is defined as the standard deviation of $V_{TH}$ difference between PMOS and NMOS transistors as defined in (20), is normalized by the nominal value in this process. $V_{DD_{min}}$ can be well estimated by the model within 11% error. The model does not depend on manufacturing technologies, because the model is derived from the subthreshold characteristics of MOSFET. $V_{DD_{min}}$ of the inverter chain in a 40nm CMOS process is shown in Fig. 9. $V_{DD_{min}}$ is also obtained by the model with less than 11% error.

The closed-form expression in (37), (40) and (41) indicates that $V_{DD_{min}}$ is proportional to $\sqrt{\ln(N/2)}$. Figure 10 illustrates $V_{DD_{min}}$ of the inverter chain as a function of $\sigma_{pn}$ in 65nm process.

Next, chains consisting of various gates are examined. Let $P_{INV}(V_{DD})$ and $P_{NAND2}(V_{DD})$ be the probabilities to satisfy the condition (23) at $V_{DD}$ of an inverter and an NAND2, respectively.

$$V_{DD_{min}} = \beta_{PN} \sigma_{PN}$$

where $\beta_{PN}$ is the ratio of PMOS and NMOS transistors. The ratio of PMOS and NMOS transistors is defined as $\beta_{PN} = \frac{W_{PMOS}}{W_{NMOS}}$. In the process of the NAND2 and NOR2 gates, $\beta_{PN}$ is larger than that of the inverter gate, which results in higher $V_{DD_{min}}$ of the NAND2 chains than $V_{DD_{min}}$ of the NOR2 chains. It should be noted that the slopes of simulated $V_{DD_{min}}$ of the inverter, NAND2, and NOR2 chains are almost same as shown in Fig. 11, since they have the identical $\sigma_{PN}$ as described in Section 2.2.

Figure 11 depicts $V_{DD_{min}}$ of the NAND2 and NOR2 chains in a 65nm CMOS process. $V_{DD_{min}}$ of the NAND2 and NOR2 chains can be calculated within 10% and 5% errors, respectively. Since $\beta_{PN} > \beta_{IN}$, i.e. PMOS transistors are stronger than NMOS in this process, the NAND2 gate is more unbalanced than the NOR2 gate in (40) and (41) of the NAND2 is larger than that of the NOR2, which results in higher $V_{DD_{min}}$ of the NAND2 chains than $V_{DD_{min}}$ of the NOR2 chains. It should be noted that the slopes of simulated $V_{DD_{min}}$ of the inverter, NAND2, and NOR2 chains are almost same as shown in Fig. 11, since they have the identical $\sigma_{PN}$ as described in Section 2.2.
measured VDDmin, which is defined as the median of the measured for the NAND chain were measured. Figure 14 illustrates the observed in one chain. 20 dies for the inverter chain and 14 dies implies that VDDmin of gate chains is equivalent to V DDmin of any does not depend on the order of the gates as indicated by (42). This indicates that the difference between VDDmin obtained by the calculations and by the following two simulations; 1) inverters NAND2's are placed alternately, and the total number of the simulations 1 and 2 is small. This is because V DDmin is determined only by the kind and the number of logic gates and V DDmin does not depend on within-die and die-to-die VTH variations, respectively. The proposed model is verified with Monte Carlo simulations using various gate chains. It is revealed that V DDmin of inverter chains can be estimated by the proposed model with less than 11% error. The proposed model is also verified with the silicon measurements and the model is consistent with the measurements.

5. CONCLUSION
The closed-form expression in (37), (40) and (41) for estimating VDDmin of CMOS logic gates was proposed. V DDmin of logic gates can be expressed as a linear function of the square-root of logarithm of the number of logic gates and its slope and intercept depend on within-die and die-to-die VTH variations, respectively. The proposed model is verified with Monte Carlo simulations using various gate chains. It is revealed that V DDmin of inverter chains can be estimated by the proposed model with less than 11% error. The proposed model is also verified with the silicon measurements and the model is consistent with the measurements.

6. ACKNOWLEDGMENTS
This work was carried out as a part of the Extremely Low Power (ELP) project supported by the Ministry of Economy, Trade and Industry (METI) and the New Energy and Industrial Technology Development Organization (NEDO).

7. REFERENCES