

# An On-Chip Characterizing System for Within-Die Delay Variation Measurement of Individual Standard Cells in 65-nm CMOS

Xin Zhang, Koichi Ishida, Makoto Takamiya, and Takayasu Sakurai

University of Tokyo, 4-6-1 Komaba, Meguro-ku, Tokyo 153-8505, Japan

E-mail: zhangxin@iis.u-tokyo.ac.jp

**Abstract** - New characterizing system for within-die delay variations of individual standard cells is presented. The proposed characterizing system is able to measure rising and falling delay variations separately by directly measuring the input and output waveforms of individual gate using an on-chip sampling oscilloscope in 65nm CMOS process. 7 types of standard cells are measured with 60 DUT's for each type. Thanks to the proposed system, a relationship between the rising and falling delay variations and the active area of the standard cells is experimentally shown for the first time.

## I Introduction

With the advancement in the deep submicron CMOS technology beyond 65nm, accurate characterization and measurement of delay variation of standard cells is becoming essential for design for manufacturing, process optimization and yield enhancement [1,2].

Conventional ways of measuring the delay variation using ring oscillator or gate-chain [3-4] failed to measure single-gate contributions, because the period of ring oscillators and gate chain is determined by the sum of gate delays. Based on the directly measured waveform of individual gate by using on-chip sampling oscilloscope [5], our proposed method is able to measure the input and output waveforms of an individual gate separately, therefore enables the characterization of both rising and falling delays.

## II. On-Chip Oscilloscope for Waveform Measuring

An on-chip sampling scheme with pico-second timing resolution was presented in 90nm CMOS [5]. Based on this architecture, an on-chip sampling oscilloscope is implemented in 65nm CMOS process for on-chip waveform measuring. Fig. 1 shows the block diagram of the on-chip sampling oscilloscope, which consists of sampling timing generator (STG), reference voltage generator (a 7 bit DAC), and the sampling head (SH).

$V_{DUT}$  is repetitively sampled by the sampling head at sampling enable (SE) edge and compared with  $V_{REF}$ . By both scanning  $V_{REF}$  and the timing of SE,  $V_{DUT}$  can be converted to digital signal by comp\_head. Furthermore, any random noise introduced by the on-chip sampling oscilloscope can be reduced by averaging hundreds of reconstructed waveforms.

## III. Implementation of On-Chip Characterizing System

Based on the above oscilloscope, an on-chip characterizing system for individual standard cells is presented in Fig. 2. For

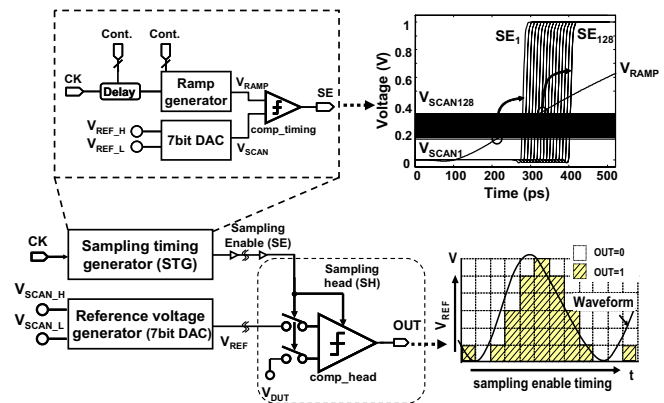


Fig. 1. Block diagram of on-chip sampling oscilloscope.

each type of standard cell (shown as a NAND2 gate for example), 60 duplicates of DUT's and SH's are implemented. The number of DUT's and SH's is chosen by a trade off of adequate number to show distribution, total available layout area, and types of standard cells to be measured.

Same comparator (comp\_head) is used for measuring both input and output waveform, thus the offset from comparator can be cancelled out. A rise-fall controller is implemented to apply rising or falling edge of excitation (EX) signal to the DUT. The oscilloscope controller is shared among all the 60 DUT's and SH's in order to minimize the variation introduced by the controlling circuit. Inverters are employed as input and output load to DUT, as a common fan-out 4 situation in a real digital system.

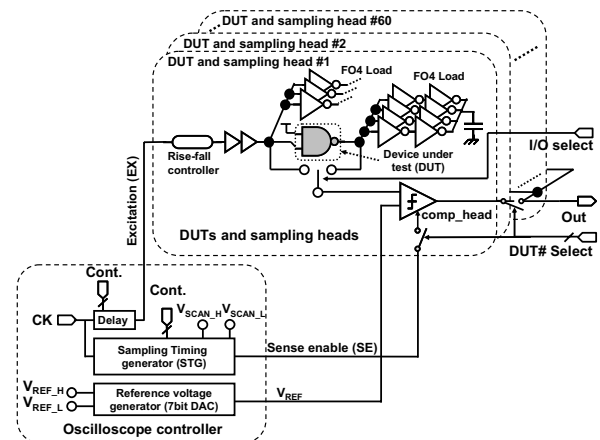


Fig. 2. Circuit schematic of within-die delay variation measurement using on-chip sampling oscilloscope.

The test chip is fabricated in 65nm CMOS process. Fig. 3 shows the chip microphotograph and the layout. 7 types of standard cells: INVx1, INVx2, INVx4 (named by increasing drivability), NAND2, NOR2, NAND3, and NOR3 are measured with 60 DUT's for each. The total 420 DUT's and 420 sampling heads consume an area of 1200 $\mu\text{m}$  $\times$ 1500 $\mu\text{m}$ , and the oscilloscope controller occupies 280 $\mu\text{m}$  $\times$ 780 $\mu\text{m}$ .

IV. Measurement Results and Analysis

The noise due to on-chip sampling oscilloscope can be reduced by averaging several reconstructed waveforms. In this study, each waveform is sampled 190 times and averaged to suppress random noise introduced by the sampling oscilloscope.

Fig. 4 shows the measured rising and falling delays. (In this paper, rising/falling delay is also referred as  $t_{pLH}/t_{pHL}$ , which means the propagation delay with a low-to-high/high-to-low transition in the output.) As we expected, in the rising/falling transition, NOR3/NAND3 is observed to be the slowest, because there are 3 PMOS's/NMOS's in series from output to power/ground.

Fig. 5 shows the sigma  $t_p$ /average  $t_p$  ( $\sigma_{t_p}/\mu_{t_p}$ ), the x-axis is chosen to be  $1/\sqrt{\text{Active area } (\mu\text{m}^2)}$ , where active area means the total gate area of transistors which are on the conducting path at rising and falling transition, respectively.

As well known, for rising and falling output, the transition is a result of conduction through the devices in the path from output to the power or ground rail. Therefore, for a rising/falling output, the PMOS/NMOS on the transition path will be the significant contributors to the delay variation. Thus,

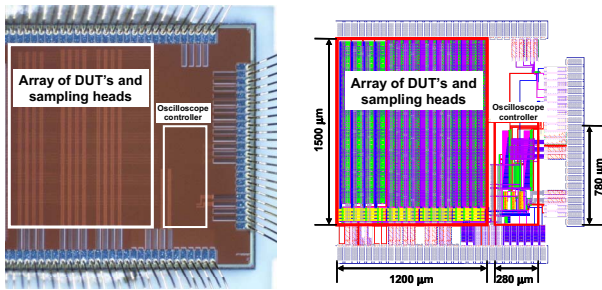


Fig. 3. Photo and layout of the test chip.

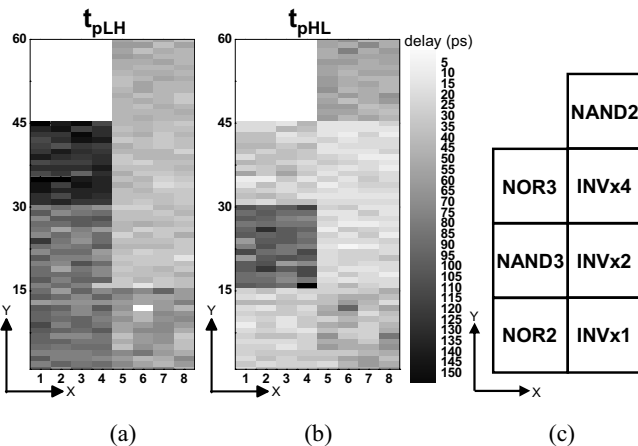


Fig. 4. Within-die delay distribution of (a)  $t_{pLH}$ , (b)  $t_{pHL}$ , (c) actual layout of DUT's corresponding to (a) and (b).

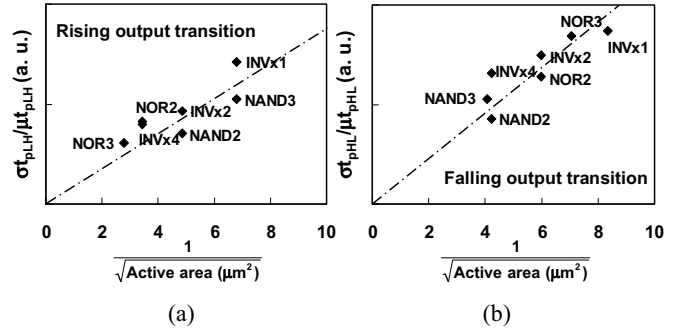


Fig. 5. Measured sigma  $t_p$ /average  $t_p$  ( $\sigma_{t_p} / \mu_{t_p}$ ) with (a) rising output transition, and (b) falling output transition.

because  $t_{pLH}$  and  $t_{pHL}$  are mixed in conventional methods, the dependency of  $\sigma_{t_p}/\mu_{t_p}$  on active area shown in Fig. 5 is impossible to be measured. By measuring  $t_{pLH}$  and  $t_{pHL}$  separately, such dependency is shown for the first time.

V. Conclusion

An on-chip characterizing system for within-die delay variations measurement of individual standard cells is proposed and fabricated. Thanks to the proposed scheme, a relationship between the rising and falling delay variation and the active area is experimentally shown for the first time.

Acknowledgments

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