A Charge-Domain Auto- and Cross-Correlation Based IR-UWB Receiver with Power- and Area-efficient PLL for 62.5ps Step Data Synchronization in 65nm CMOS

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Abstract

A 100Mb/s, 1.71mW DC-960MHz band impulse radio ultra-wideband (IR-UWB) receiver is developed in 1.2V 65nm CMOS. A novel auto- and cross-correlation based synchronization scheme is proposed to achieve 62.5ps step data synchronization with a 2-GHz 8-phase PLL clock generator. The developed UWB receiver with the proposed power- and area-efficient PLL achieves the low energy consumption of 17.1pJ/bit.

Introduction

Correlation-based receivers [1] attain superior noise performance and robust narrowband interference suppression at the expense of increased power consumption and increased circuit complexity over their thresholding-based counterparts [2]. To reduce the power consumption of the correlation-based receiver, a 1.28mW 100Mb/s UWB receiver with charge-domain correlator and embedded sliding scheme for data synchronization is developed in [1] where there is an inherent assumption that the timing mismatch between the incoming signal and the template of the correlator is zero when the synchronization is achieved. Fig. 1 shows the simulated BER dependency on timing mismatch. When the timing mismatch is reduced from 500ps to 62.5ps, E_b/N_0 can be improved by 7.8dB for the white noise and 5.8dB for the narrowband interference.

To achieve 62.5ps timing mismatch, a 16-GHz PLL clock generator and high resolution comparators are required in the conventional topology [1] and the receiver power consumption will be increased by eight times. This work aims to minimize this power consumption with 2-GHz 8-phase PLL clock generator by a novel auto- and cross-correlation based synchronization scheme. To further reduce the power consumption of the capacitance multiplier used in the conventional area-efficient PLL [3], a dual charge-pump PLL is proposed to scale up the capacitance of the loop filter without extra charge-pump current.

Synchronization Scheme

The architecture of the proposed IR-UWB receiver is shown in Fig. 2. It consists of one dual charge-pump PLL for multi-phase clock generation and two coupled delay-locked loops (DLL) for coarse and fine timing alignment. Fig. 3 shows the correlator output dependency on timing mismatch ΔT between the signal and the templates of the correlators.

Data synchronization is achieved in two steps. When the timing mismatch ΔT is larger than 0.5ns, the upper coarse timing alignment loop is activated and the incoming signal is auto-correlated with a stored replica of the signal shape. The upper loop can keep sliding the phase of the sampling clock with the conventional unidirectional sliding scheme until the auto-correlation result V_{cor1} is higher than the threshold of the comparators. When the timing mismatch is equal to or less than 0.5ns, the lower fine timing alignment loop is activated and the incoming signal is cross-correlated against a stored replica of the derivative of the signal pulse shape. This loop can keep switching the multi-phase output of the PLL until the timing mismatch ΔT is less than 62.5ps.

The incoming BPSK-modulated Gaussian first-order derivative pulse and the discrete templates for the auto- and cross-correlators are shown in Fig.4 (a). The bandwidth of the incoming pulse is from DC to 960MHz and it is sampled at the rate of 2GSa/s. The charge-domain sampling correlator in [1] is used for the auto-correlation directly. The derivative operation in the cross-correlator can be implemented by changing the values of the template capacitances and reconfiguring the addition and the subtraction circuits. Fig. 4(b) and Fig. 4(c) show the circuit schematics for the cross-correlator in sampling mode and summing mode. The control units for coarse and fine tuning loops are shown in Fig.5 (a) and Fig.5 (b), respectively. Fig. 6 shows the timing chart for the entire synchronization process. In the worst case data synchronization can be finished within nineteen phase slides and four phase switches.

Dual Charge-Pump Phase-Locked Loop

Multi-phase PLL is a critical component for the sampling clock generation in the proposed UWB receiver. The loop filter of the PLL is a barrier in fully integrating the receiver because of its large integrating capacitor. To reduce the chip area of the PLL, a capacitance multiplier is proposed to scale up the on-chip capacitor in [3]. The capacitance multiplier can be simplified to the dual charge-pump architecture in Fig. 7(a) noting that the capacitance C_p often remains below C_z by roughly a factor of 15 and thus the current flowing through C_p can be neglected. This architecture reduces the chip area at the cost of an extra $(1-1/k)I_p$ charge-pump current consumption, where k is the capacitance scaling factor and I_p is the normal charge-pump current. This extra charge-pump current can be eliminated by reversing the order of the resistor and the capacitor in the filter and biasing the filter to $V_{DD}/2$. As shown in Fig. 7(b), the total current of the two charge-pumps is reduced to the normal value I_p while the capacitance is multiplied by k times. In this work k is equal to 8 and a 28pF capacitance is scaled up to 224pF.

Experimental Results

The proposed UWB receiver without the front-end amplifier was designed and fabricated in 1.2V 65nm CMOS process. The chip micrograph and layout are shown in Fig. 8 . Power consumption and area occupation are summarized in Table I. Loop stability of the proposed dual charge-pump PLL can be verified by measuring the VCO control voltage in Fig. 9 (a). Figure 9 (b) shows the measured jitter of 1.33ps (rms) and 15.76ps (peak-to-peak). To verify the fine-tuning time step, the phase-switching loop with cross-correlation was measured separately. As show in Fig.10 (a), with each left or right shifting control signal, the sampling clock period is increased or decreased by 62.5ps from 10ns. Fig.10 (b) shows the measured waveforms when the synchronization is achieved. The comparison with the state-of-the-art correlation-based IR-UWB receivers is shown in Table II. The proposed UWB receiver with the area- and power-efficient PLL achieves the energy consumption of 17.1pJ/bit with the 62.5-ps timing step for data synchronization.

Acknowledgment

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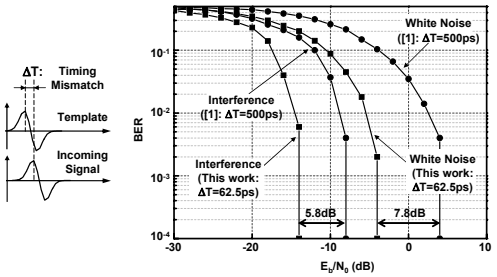


Fig. 1. Simulated BER dependency on timing mismatch (ΔT).

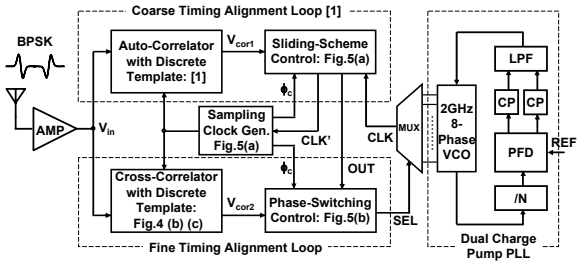


Fig. 2. Proposed IR-UWB receiver with dual charge-pump PLL.

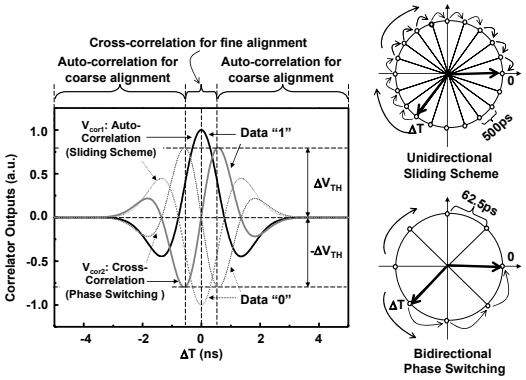


Fig. 3. Dependence of correlator output on timing mismatch (ΔT) for auto- and cross-correlation.

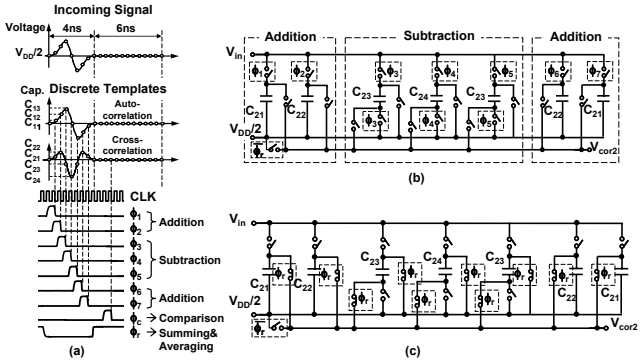


Fig. 4. (a) Incoming signal and templates. (b) Cross-correlator in sampling mode. (b) Cross-correlator in summing and averaging mode.

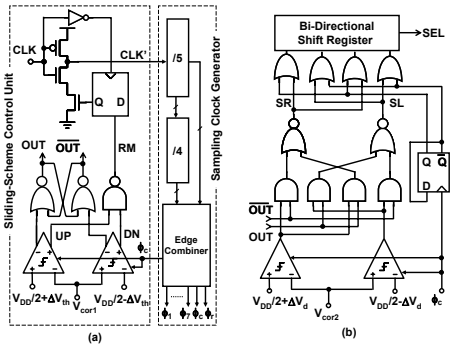


Fig. 5. (a) Sliding-scheme control unit and sampling clock generator. (b) Phase-switching control unit.

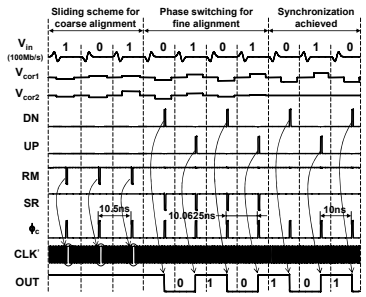


Fig. 6. Timing chart for coarse and fine timing alignment.

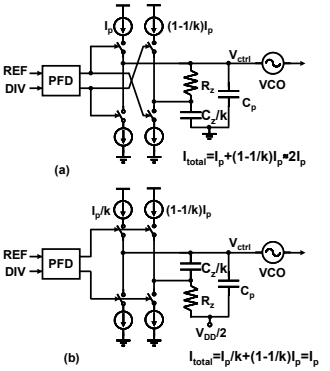


Fig. 7. Dual charge-pump PLL. (a) Conventional topology. (b) Proposed topology.

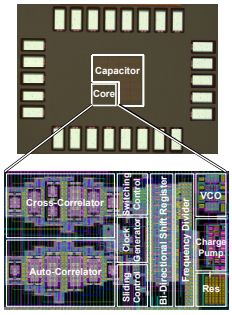
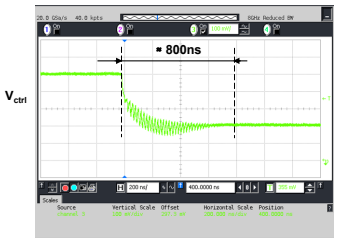


Fig. 8. Chip micrograph and layout.

Table. I
Performance summary.

PLL Power (mW)	Charge Pump	0.48
	VCO	0.52
	Divider &PFD	0.12
	Total	1.12
Coarse & Fine Tuning Loop Power (mW)		0.59
Total Power (mW)		1.71
Energy per bit (pJ/bit)		17.1
Area (μm^2)	Capacitance	49900
	Core	9200



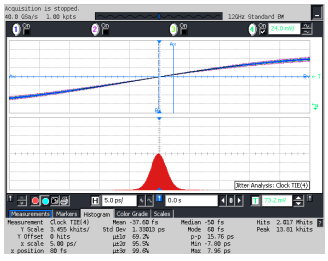


Fig. 9. Measurement results for PLL. (a) Measured VCO control voltage for frequency jump. (b) Measured PLL output jitter.

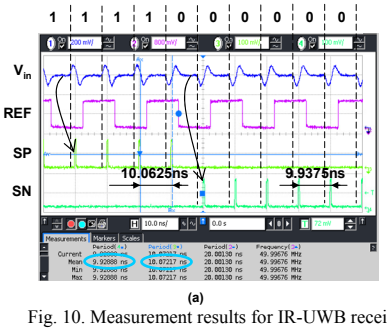


Fig. 10. Measurement results for IR-UWB receiver. (a) Phase switching for fine timing alignment. (b) Measured waveforms in synchronization.

Table. II Comparison with state-of-the-art correlation-based IR-UWB receivers.

		ISSCC'06 [4]	ISSCC'06 [5]	ISSCC'09 [6]	This Work
Technology (CMOS)		0.18μm	0.18μm	0.13μm	65nm
Supply Voltage		1.8V	1.8V	1.2V	1.2V
Data Rate		400 Mb/s	20 Mb/s	40 Mb/s	100 Mb/s
Frequency Band		3-10GHz	3-10GHz	0-960MHz	0-960MHz
Timing Step	Coarse	1ns	1ns	NA	500ps
	Fine	100ps	60ps	800ps	62.5ps
Power Consumption		81mW (with front-end)	11.1mW (w/o front-end)	2.5mW (w/o front-end)	1.71mW (w/o front-end)
Energy per bit		202.5pJ/bit	555pJ/bit	62.5pJ/bit	17.1pJ/bit